KyloRen 13" Schematics
KabyLake-R

2017-06-29

REV : -1

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Core Design>

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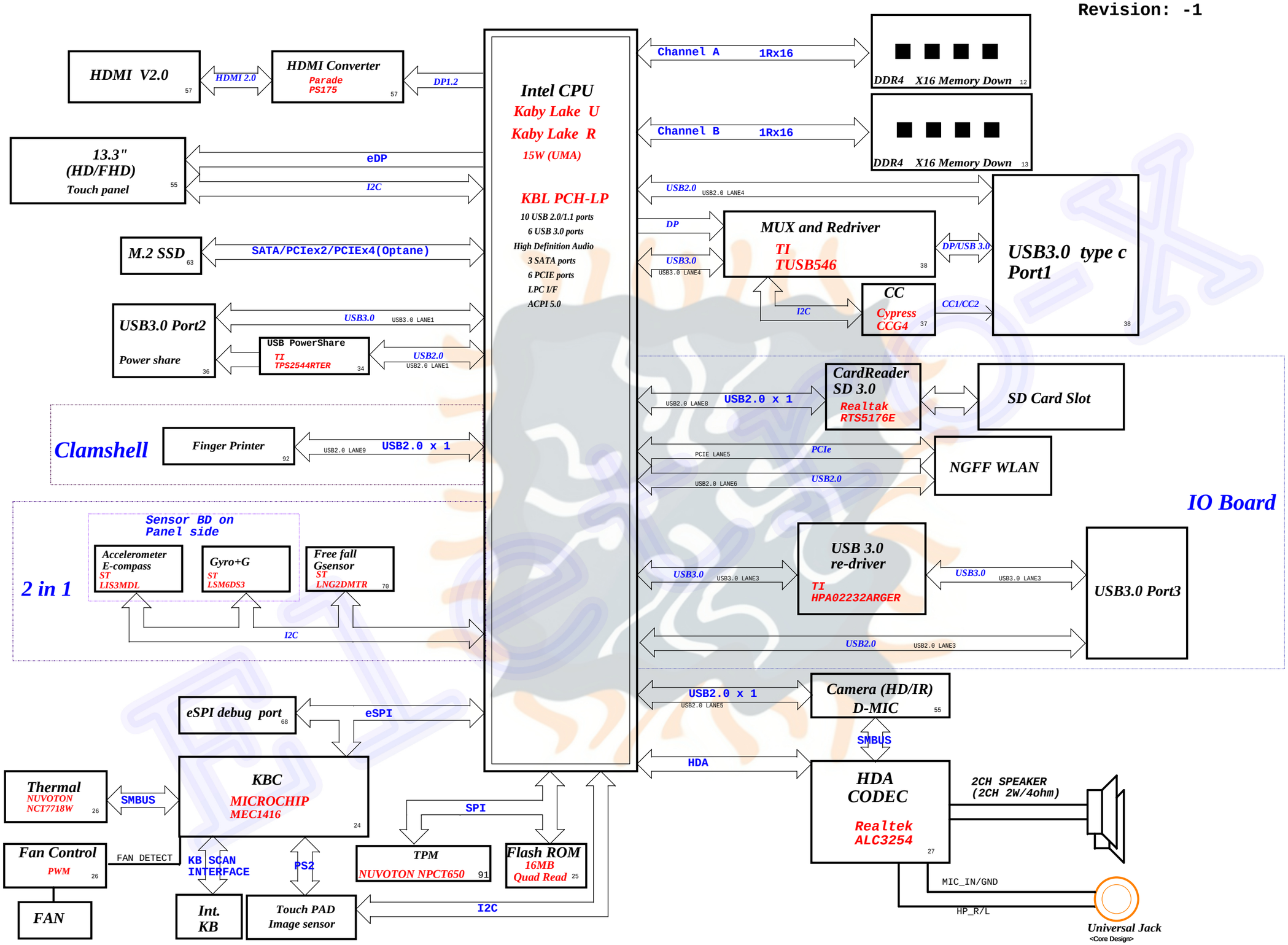
Title: *Cover Page*		
Size: A3	Document Number: KyloRen 13"	Rev: A00
Date: Thursday, June 29, 2017	Sheet 1 of 106	

Eletro-X

KBL-U(R) 13" CPU 15W Block Diagram

Project code: 4PD0B5010001
PCB P/N: 16839
Revision: -1



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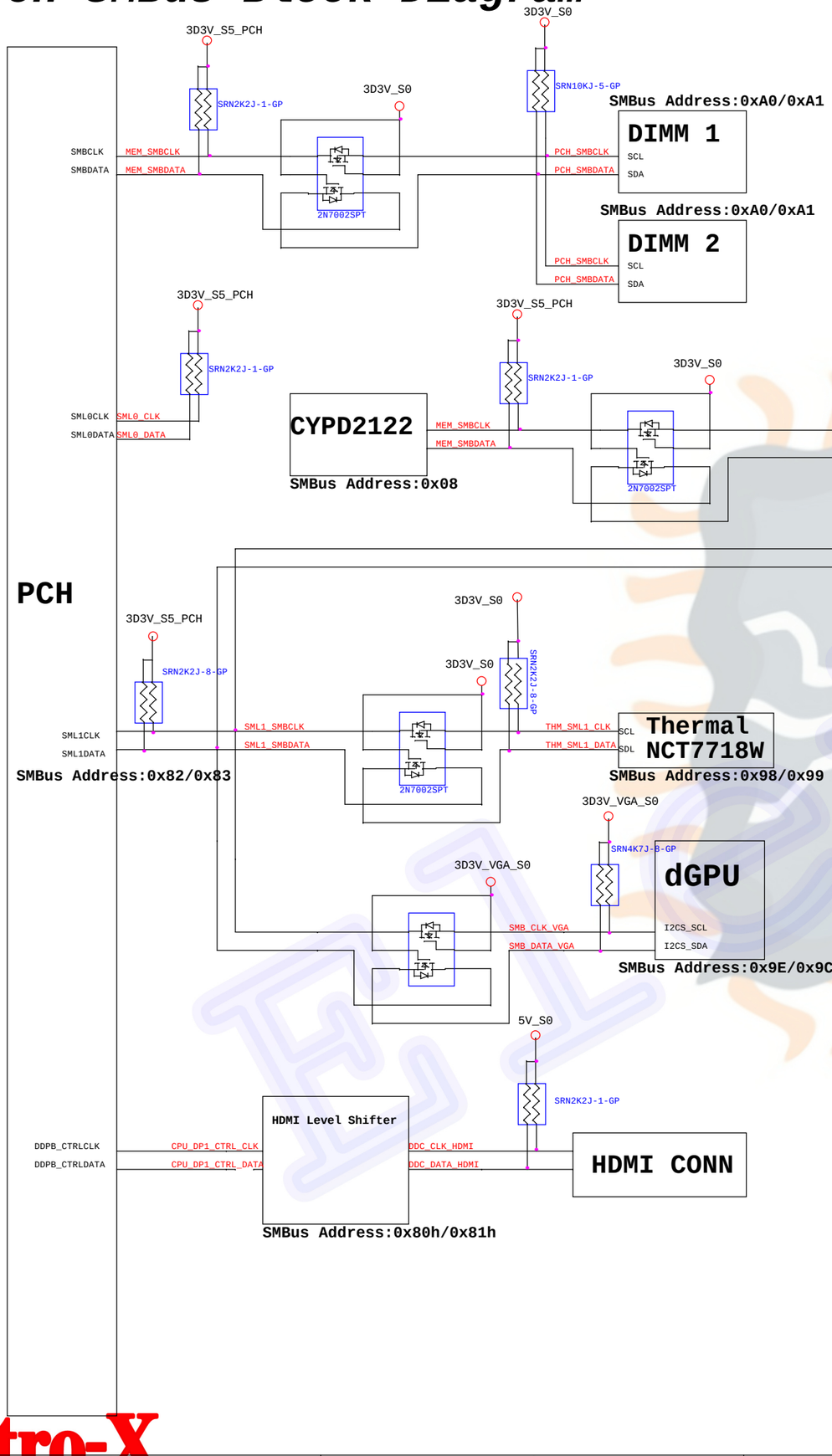
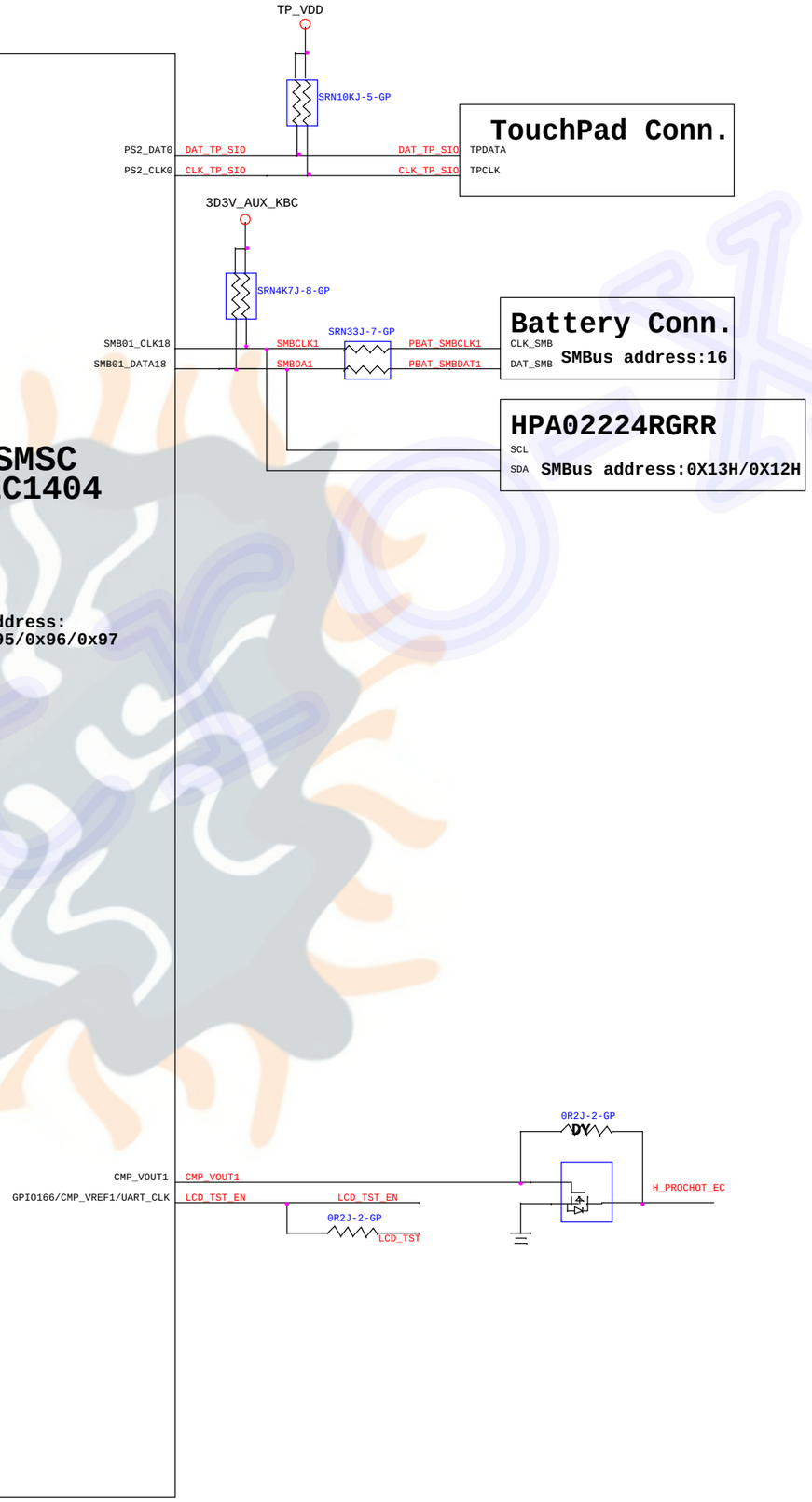
Title			
Block Diagram			
Size: C	Document Number: KyloRen 13"		Rev: A00
Date: Thursday, June 29, 2017	Sheet 2 of 106		

Eletro-X

PCH SMBus Block Diagram



KBC SMBus Block Diagram



Eletro-X

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Title: SMBUS Block Diagram
Size: A2
Document Number: KyloRen 13"
Rev: A00
Date: Thursday, June 29, 2017
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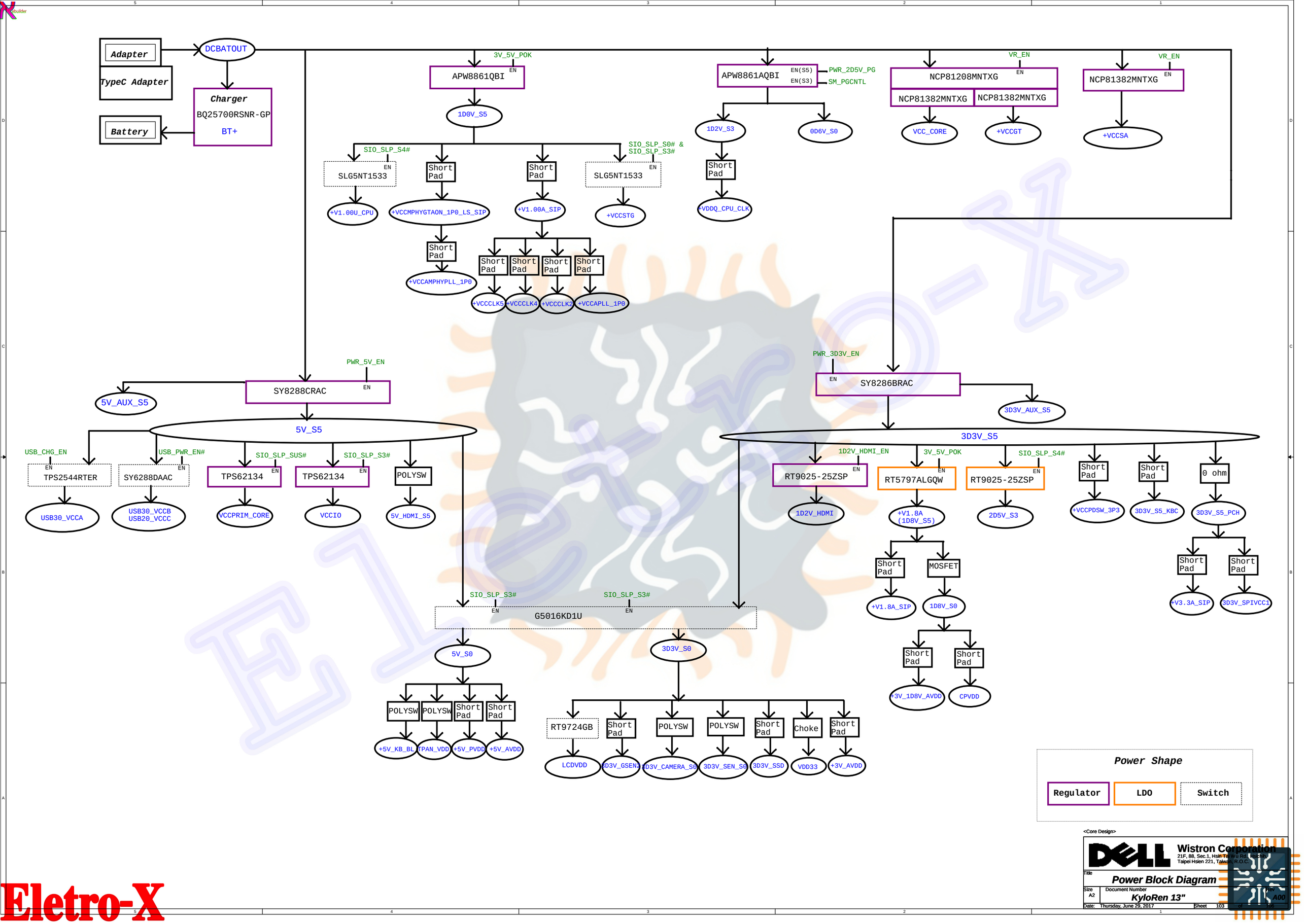

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Title: Power Block Diagram

Size: A2 | Document Number: KyloRen 13" | Rev: A00

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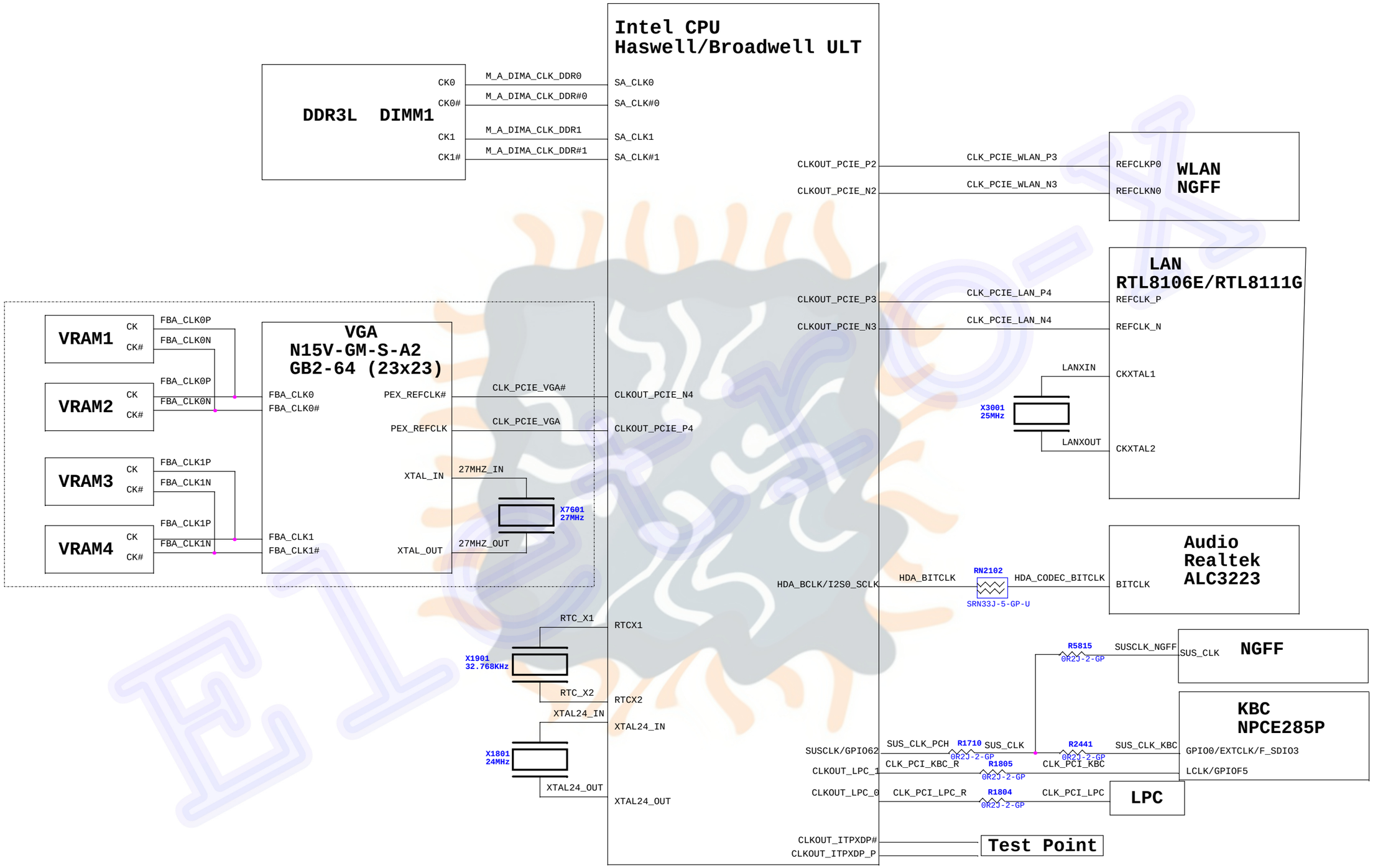
Eletro-X

CLK Block Diagram



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Title: CLK Block Diagram

Size: A2 | Document Number: KyloRen 13" | Rev: A00

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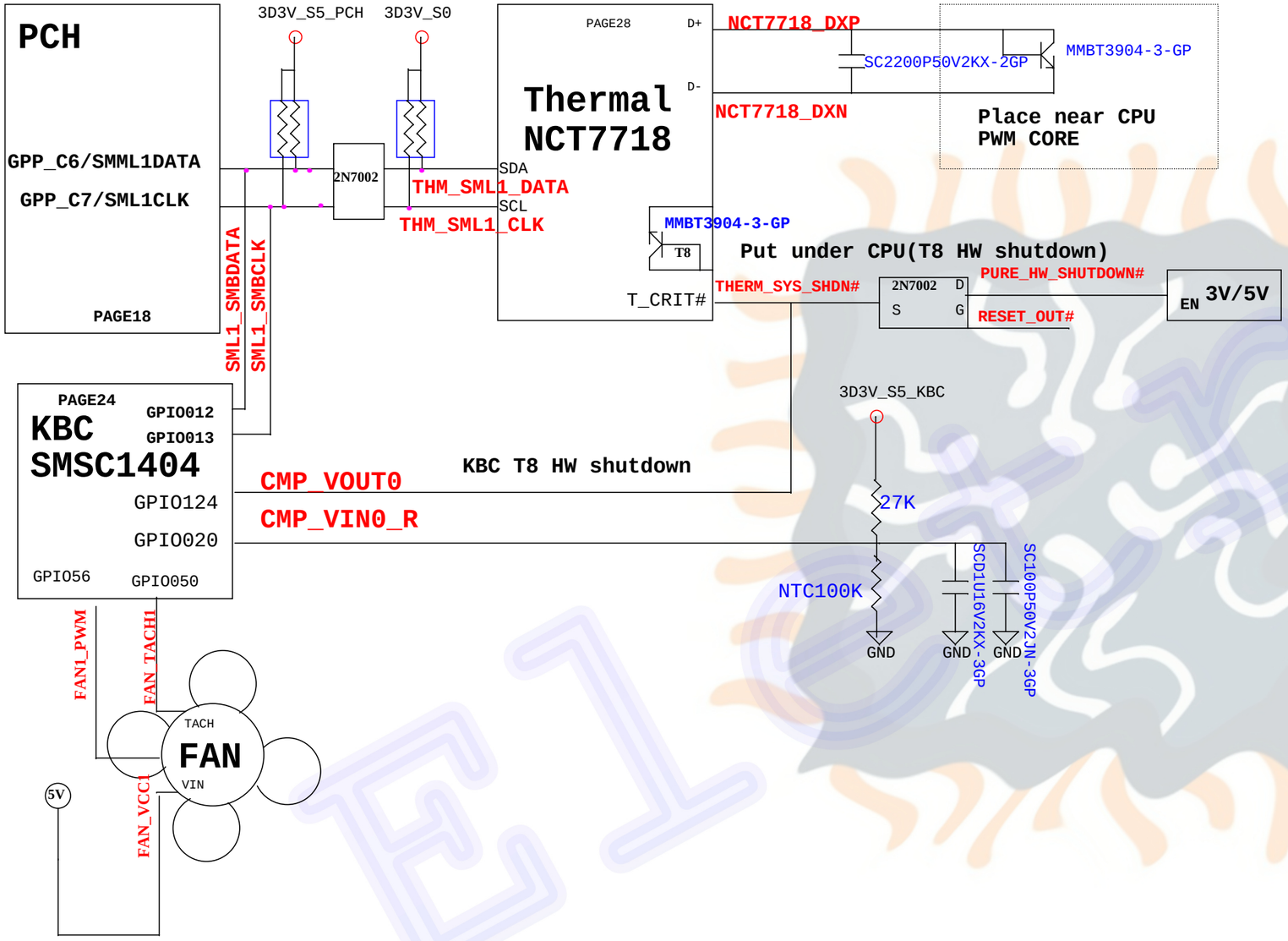
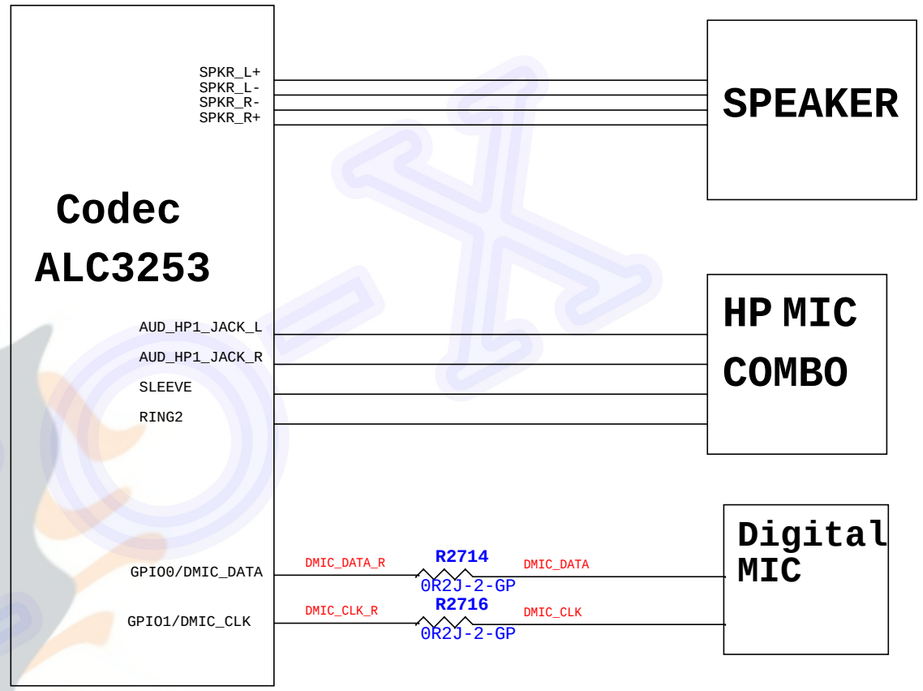
Eletro-X

Thermal Block Diagram



Audio Block Diagram



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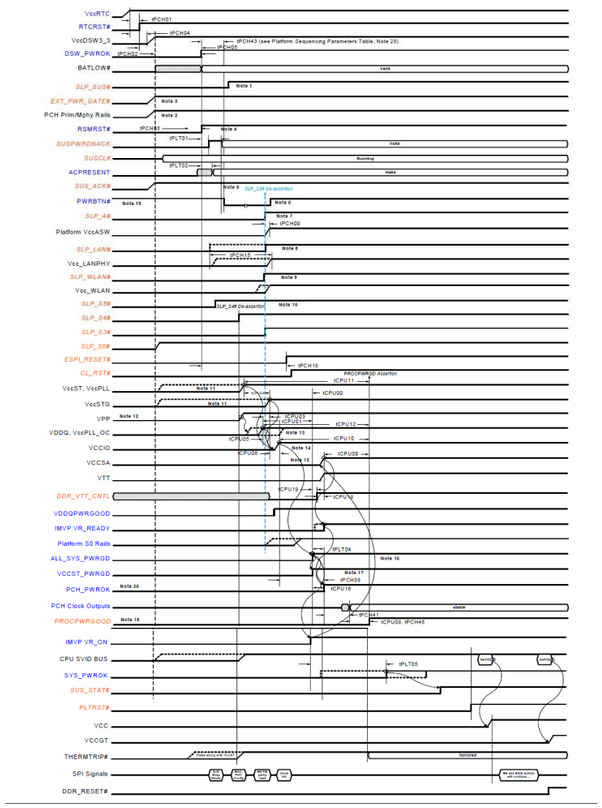
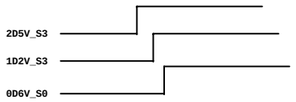
Title	Thermal/Audio Block Diagram	
Size: Custom	Document Number: KyloRen 13"	Rev: A00
Date: Thursday, June 29, 2017	Sheet 105 of 108	

Eletro-X

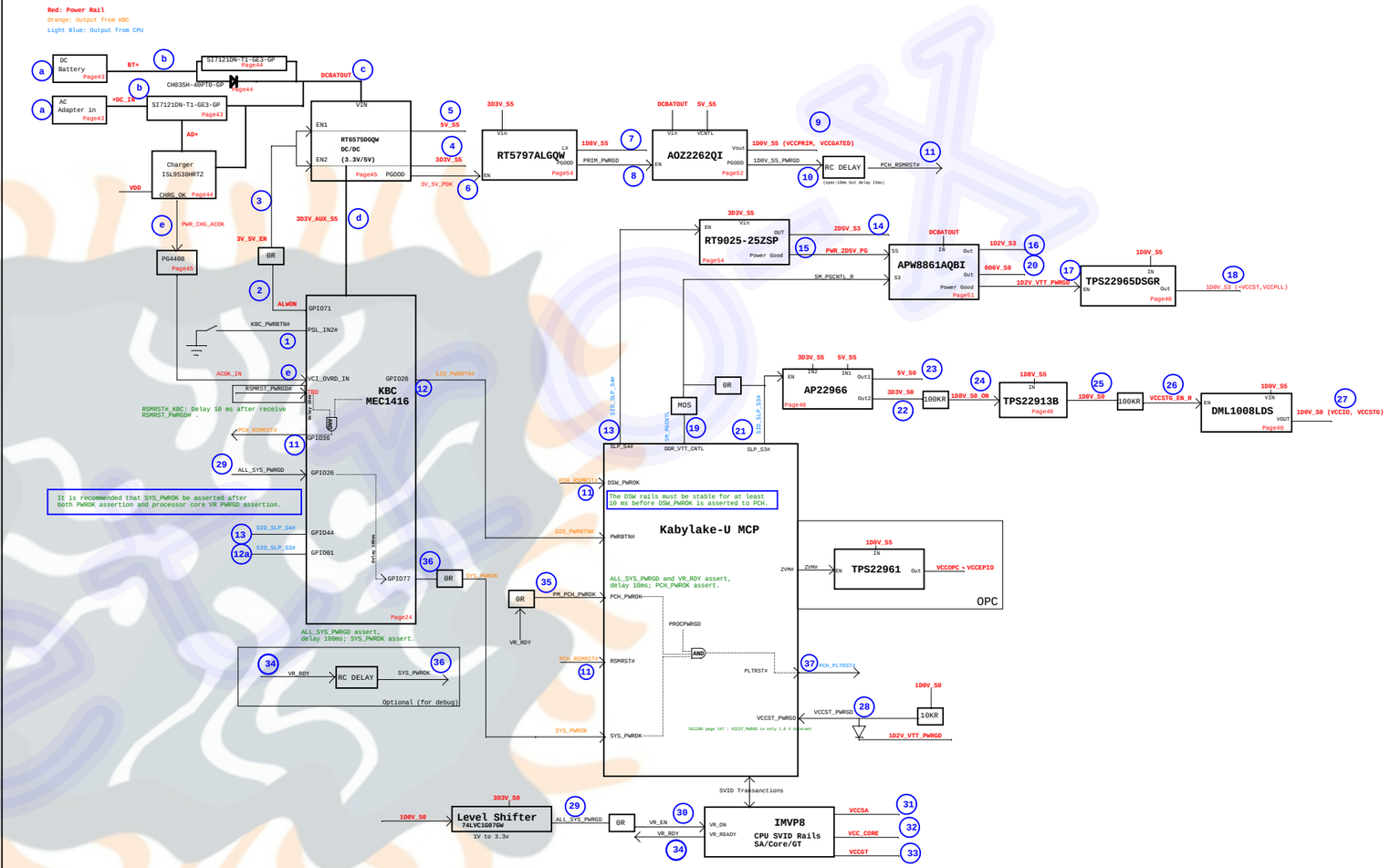
SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



For DDR4 power sequence



Kabylake POWER UP SEQUENCE DIAGRAM (Non-Deep Sx Platform)



a → b → c → d → e

1 → 2 → 3 → 4 → 5 → 6 → 7 → 8 → 9 → 10 → 11 → 12 → 13 → 14 → 15 → 16 → 17 → 18 → 19 → 20 → 21 → 22 → 23 → 24 → 25 → 26 → 27 → 28 → 29 → 30 → 31 → 32 → 33 → 34 → 35 → 36 → 37

Eletro-X

SSID = CPU

#544669 CRB Rev0.52

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

+VCCSTG = 1.0 V

+VCCSTG = 1.0 V

+VCCST_CPU

R419 1KR2J-1-GP

PCH_THERMTRIP#

EC401 AZ5725-01FDR7G-GP DY

20160812 EMI

+VCCSTG

R401 1KR2J-1-GP Rb

R403 499R2F-2-GP Ra

24 PECI
24,44,46 H_PROCHOT#

TP401 TPAD14-OP-GP

TP402 TPAD14-OP-GP

H_CATERR#
H_PROCHOT# R
PCH_THERMTRIP#
SKTOCC#

CPU1D

4 OF 20

SKYLAKE_ULT

CATERR# D63
PECI A54
PROCHOT# C65
THERMTRIP# C63
SKTOCC# A65

CPU MISC

BPM#[0] C55
BPM#[1] D55
BPM#[2] B54
BPM#[3] C56

99 XDP_BPM0
99 XDP_BPM1
XDP_BPM2
XDP_BPM3

TP407 TPAD14-OP-GP
TP408 TPAD14-OP-GP

TP403 TPAD14-OP-GP

55 TOUCH_PANEL_INTR#

GPP_E3/CPU_GP0 A6
GPP_E7/CPU_GP1 A7
GPP_B3/CPU_GP2 BA5
GPP_B4/CPU_GP3 AY5

TOUCH_PAD_INTR#

55 TOUCH_PANEL_PD#

3D3V_S5_PCH

R404 DY 100KR2J-1-GP

CPU_POPIRCOMP AT16
PCH_POPIRCOMP AU16
EDRAM_OPIO_RCOMP H66
EOPIO_RCOMP H65

49D9R2F-GP R412
49D9R2F-GP R413
49D9R2F-GP R414
49D9R2F-GP R415

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

SKYLAKE-U-GP

071.SKYLA.000U

JTAG

PROC_TCK B61 XDP_TCK_JTAGX
PROC_TDI D60 PCH_JTAG_TDI
PROC_TDO A61 PCH_JTAG_TDO
PROC_TMS C60 PCH_JTAG_TMS
PROC_TRST# B59 XDP_TRST#

PCH_JTAG_TCK B56
PCH_JTAG_TDI D59
PCH_JTAG_TDO A56
PCH_JTAG_TMS C59
PCH_TRST# C61
JTAGX A59

PCH_JTAG_TCK 99
PCH_JTAG_TDI 99
PCH_JTAG_TDO 99
PCH_JTAG_TMS 99
XDP_TRST# 99
XDP_TCK_JTAGX 99

GP

PCH_JTAG_TDI 1 51R2J-2-GP XDP R408
PCH_JTAG_TDO 1 XDP
PCH_JTAG_TMS 100R2F-L1-GP-U 1 51R2J-2-GP XDP R409 R416

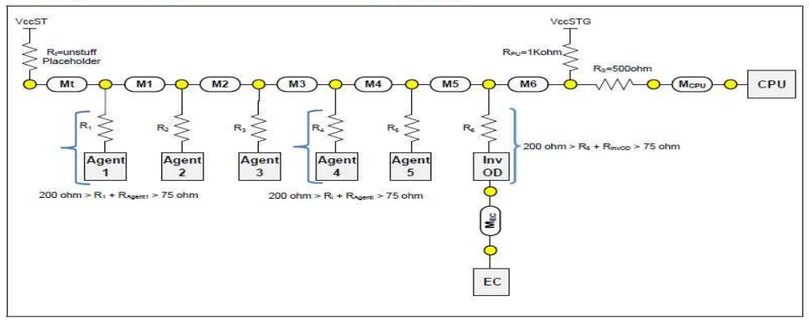
XDP_TCK_JTAGX R417 1 2 51R2J-2-GP XDP
XDP_TRST# R402 1 DY 2 51R2J-2-GP
PCH_JTAG_TCK R407 1 DY 2 51R2J-2-GP

24,65 TP_WAKE_KBC# R410 1 2 0R0402-PAD

2016/12/28

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: CPU_(JTAG/CPU SIDE BAND)

Size: A3 | Document Number: KyloRen 13" | Rev: A00

Date: Thursday, June 29, 2017 | Sheet 4 of 106

Eletro-X

SSID = CPU

DDR4 ball type: Non-Interleaved Type

Figure 4-40. KBL U DDR4 x8 Memory Down Placement and Block Diagram

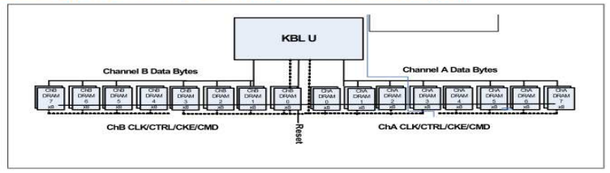
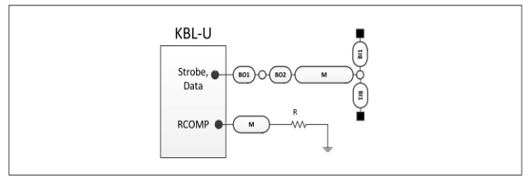
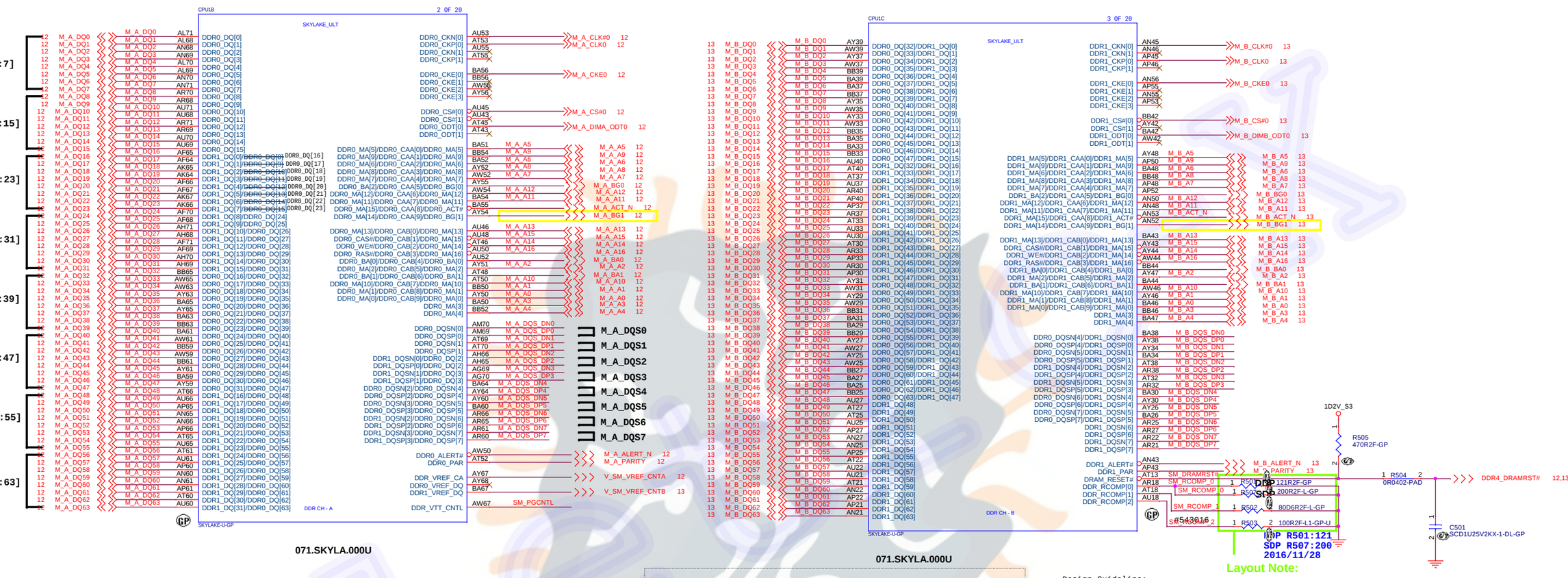


Figure 4-42. KBL U DDR4 x8 Memory Down DQ/DQS/RCOMP Signals





DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

Table 4-48. ODT Signals Connectivity Table (Sheet 2 of 2)

Processor	Memory type	Side	Signal	Rule	Notes
KBL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
	DDR3L Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
		DRAMs	ODT[1:0]		
	DDR3L SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DIMMs ODT[1:0].	1,3
		DIMMs	ODT[1:0]		
	DDR3L Mixed Memory Down and SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's SODIMM Channel ODT[1:0] connected to DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If rank1 not used, ODT[1] not connected.	3,4
		DIMM	ODT[1:0]		
		DRAMs	ODT[1:0]		
	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.	
		DRAMs	ODT[1:0]		
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.	
		DIMMs	ODT[1:0]		

Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP3 - KBL-Y LPDDR3, RVP5 - KBL-U LPDDR3, RVP7 - KBL-U DDR3L SODIMM)
2. LPDDR3 Rank1 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active). RTT NOM is defined by BIOS as High-Z in both ranks. when a Rank receives write command it enables RTT WR (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z)
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SDP dual sided and 2Rx8 dual side.

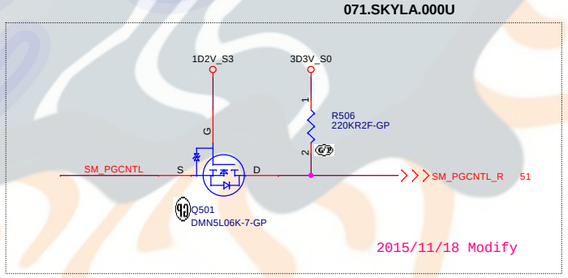
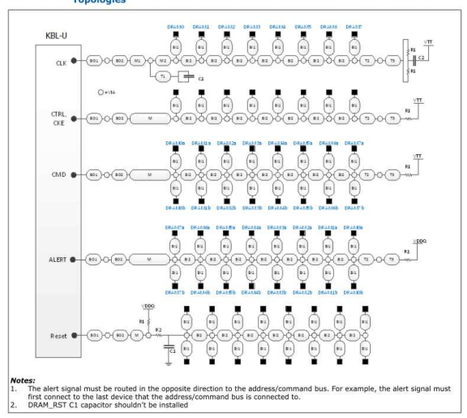


Figure 4-41. KBL U DDR4 x8 Memory Down CLK/CKE/CMD/CTRL/ALERT/Reset Signals Topologies



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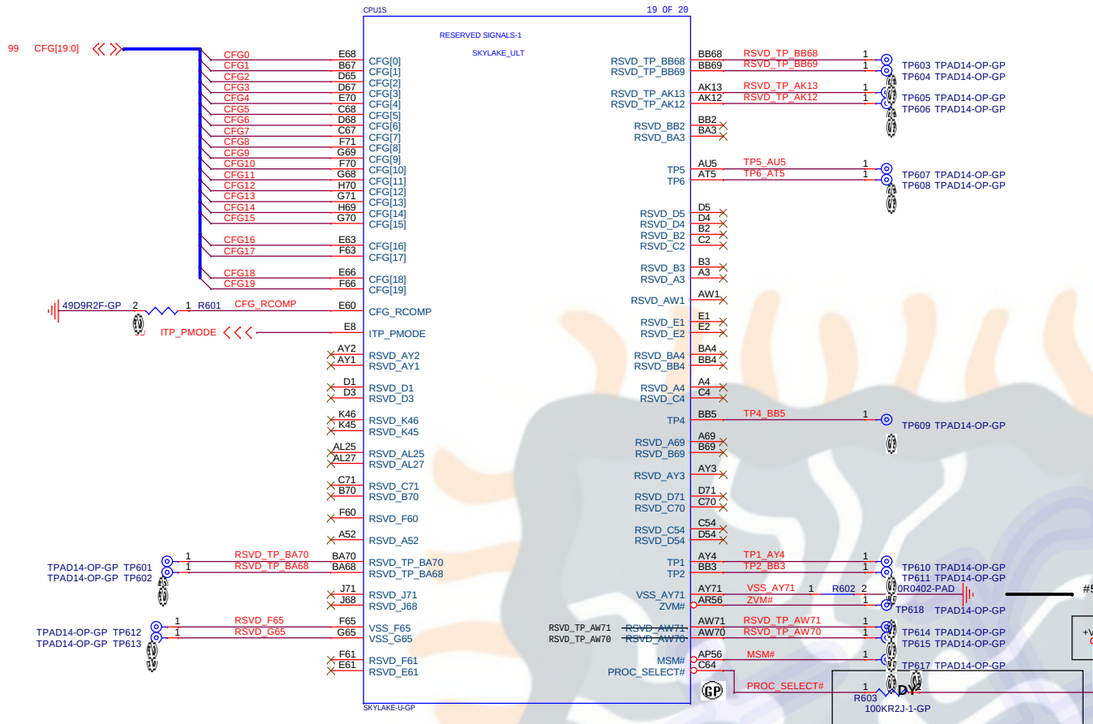
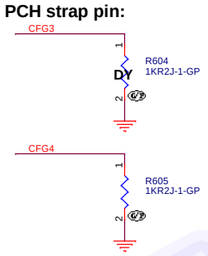
Title	CPU (DDR)		
Size: A2	Document Number: KyloRen 13"		Rev: A00
Date: Thursday, June 29, 2017	Sheet 5	of	56

ElecFA

SSID = CPU



PCH strap pin:



071.SKYLA.000U

[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

Eletro-X

SSID = CPU

3A +V_EDRAM_VR

140mA +V1.8S_EDRAM

SEN_EDRAM

3A +V_EOPIO_VR

SEN_EOPIO

071.SKYLA.000U

For U22 & U42

For U42 only

2017/01/18

2017/06/28

#544669 CRB.

2016/02/16 modify

Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

SVID_543016:

SVID DATA

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID CLOCK

Figure 10-7. Routing Illustration for SVID Topology

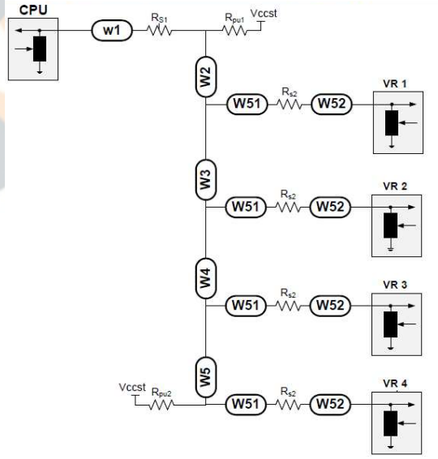
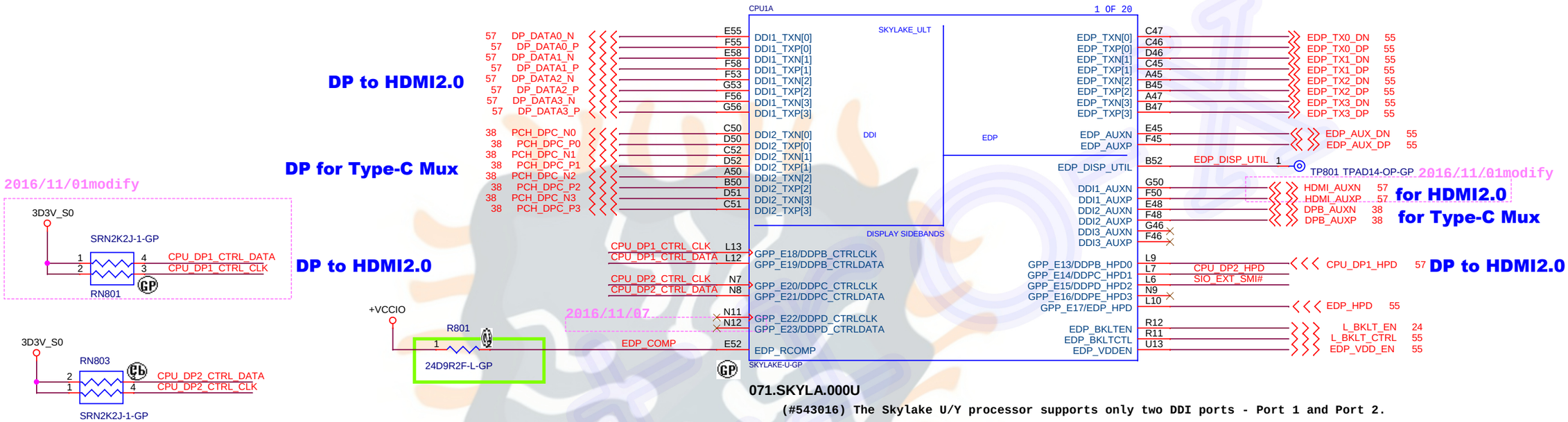


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{BT} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

Eletro-X

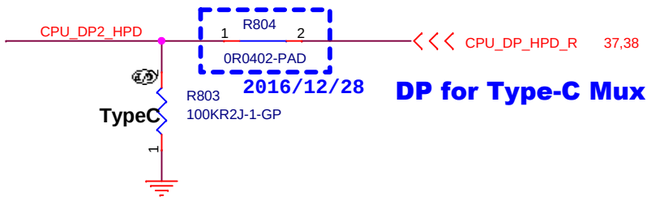
SSID = CPU



071.SKYLA.000U

(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

2016/11/07
Touch_panel _Resert Remove

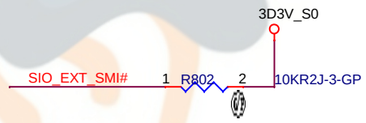


(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC



Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

<Core Design>

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Title: CPU (DISPLAY)

Size: A3 | Document Number: KyloRen 13" | Rev: A00

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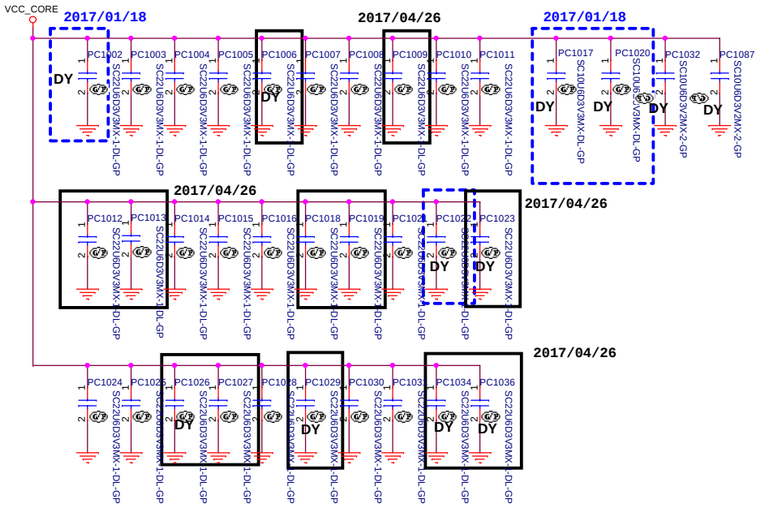
Eletro-X

SSID = CPU

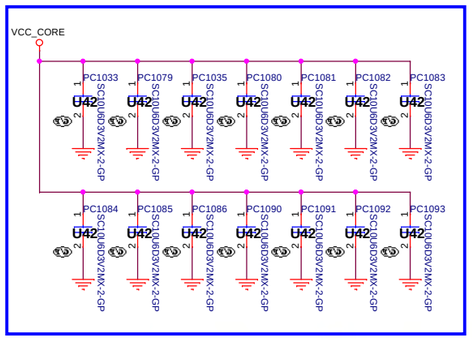
VCC_CORE

U-line 22 15W
IccMax current-10ms max = 31 A

22U 0603 x 30
10U 0402 x 2 (2DY)



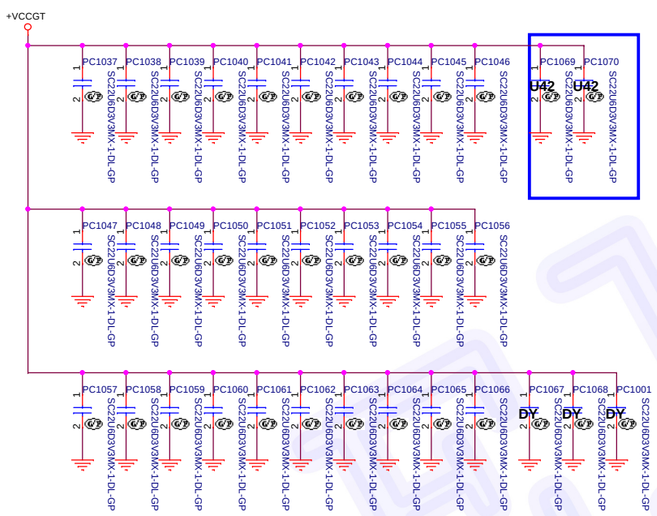
2016/11/7modify



VCCGT

U-line 22 15W
IccMax current-10ms max[A] = 64 A

22U 0603 x 30 (3 DY)



VCCSA

22U 0603 x 5 (3DY)

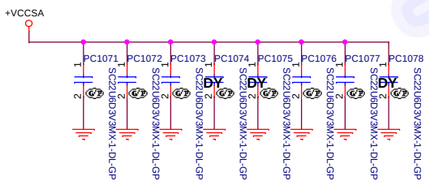


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible
		5x 22uF 0603	Additional components needed when supporting 23e
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

Table 48-5. Decoupling Requirements for Kaby Lake U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc_{EOPIO}	2x 10 uF 0402		Place on secondary side, underneath the package. Only needed when supporting 23e
Vcc_{OPC}	1x 10 uF 0402		Place on secondary side, underneath the package. Only needed when supporting 23e
	6x 1 uF 0201		
VCC (for 0.55mm Z height Solution Only) (Note 5)	27x 10 uF 0402		Place on secondary side, underneath the package
	35x 1 uF 0201		Refer to diagram in Note 3 below for placement recommendation of 0201 caps
		8x 47 uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10 uF 0402	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP1)
Size: A2 | Document Number: KyloRen 13" | Rev: A00
Date: Thursday, June 29, 2017 | Sheet 10 of 108

Eletro-X

SSID = CPU

PCH DERIVED RAILS

1D0V_S5

2017/05/08

+VCCPRIM_CORE

R1101 0R1206-PAD

+V1.00A_SIP

R1102 0R0603-PAD

C1112 SC22U6D3V3MX-1-GP DY

3D3V_S5_PCH

+V3.3A_SIP

R1103 0R0603-PAD

C1113 SC22U6D3V3MX-1-GP DY

+V1.8A

+V1.8A_SIP

R1104 0R0603-PAD

C1122 SC22U6D3V3MX-1-GP DY

+VCCIO

+VCCIO(ICCMAX.=2.73A)

C1133 C1134 C1135 SC22U6D3V3MX-1-DL-GP DY

+VCCPRIM_CORE

C1128 C1129 SC22U6D3V3MX-1-DL-GP

VCC_CORE

2017/01/17

1U 0402 x 5

C1124 C1125 C1126 C1101 C1127 SC1U10V2KX-1DLGP DY

U-line 23e 28W
IccMax current 10ms max = 34 A

UNSLICED GT

+VCCGT

C1102 C1103 C1104 C1105 C1106 C1107 SC1U10V2KX-1DLGP DY

1U 0402 x 6

Dummy : 20150123 Dummy : 20150123

+V3.3A_SIP

C1123 SC10U6D3V3MX-DL-GP DY

1D2V_S3

C1136 C1137 C1138 SC10U6D3V3MX-DL-GP

C1139 C1140 C1141 C1142 SCD1U25V2KX-1-DL-GP

C1132 C1131 C1130 SC22U6D3V3MX-1-DL-GP DY

EC1102 EC1103 SC2D2U6D3V2MX-DL-GP DY

RF request 2016/01/12 modify

VCCIO

+VCCIO

+VCCIO(ICCMAX.=2.73A)

C1108 C1109 C1110 C1111 SC1U10V2KX-1DLGP DY

+VCCMPHYGTAON_1P0(ICCMAX.=2.12A)

+VCCMPHYGTAON_1P0_LS_SIP

C1114 SC1U10V2KX-1DLGP

C1115 SC22U6D3V3MX-1-GP DY

+VCCMPHYGTAON_1P0_LS_SIP

C1116 C1117 SC1U10V2KX-1DLGP

+VCCMPHYGTAON_1P0_LS_SIP

C1118 SC22U6D3V3MX-1-GP DY

C1119 SC1U10V2KX-1DLGP

+VCCMPHYGTAON_1P0_LS_SIP

C1120 SC10U6D3V3MX-DL-GP DY

C1121 SC1U10V2KX-1DLGP

Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

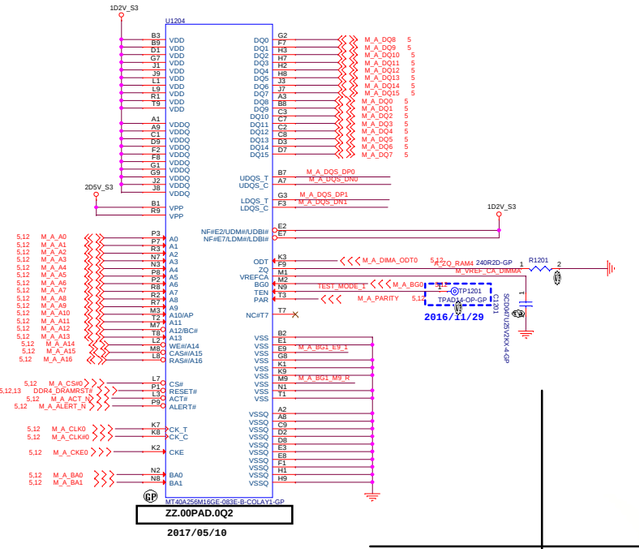
Title: CPU (Power CAP2)

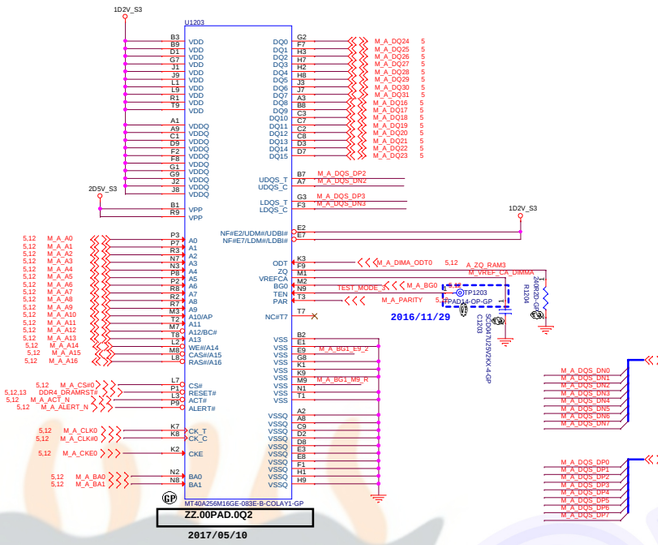
Size: A3 | Document Number: KyloRen 13" | Rev: A00

Date: Thursday, June 29, 2017 | Sheet 11 of 106

ElectrOX

SSID = MEMORY





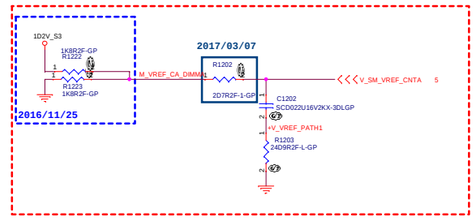
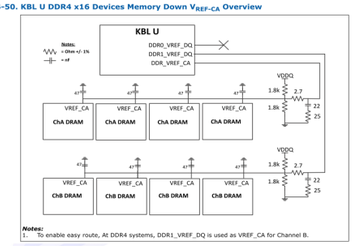
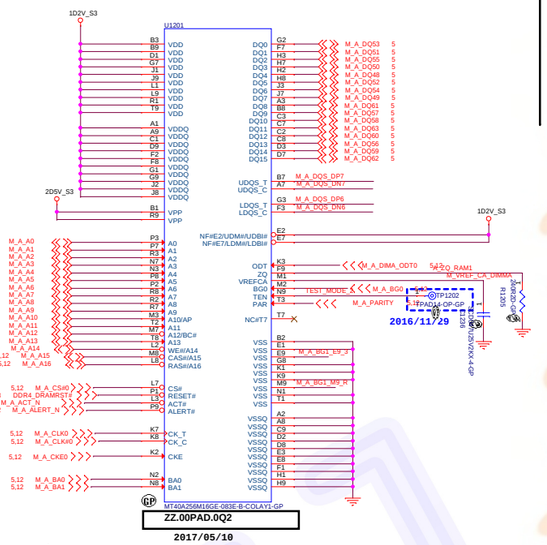
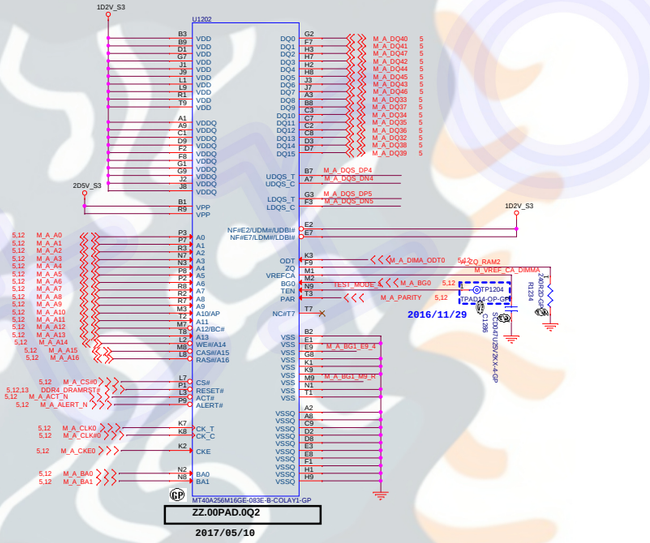
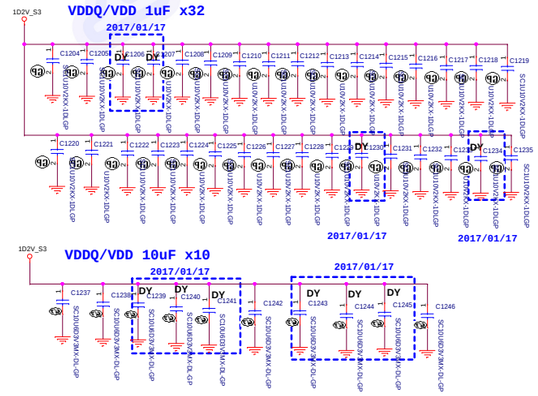


Figure 4-50. KBL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview

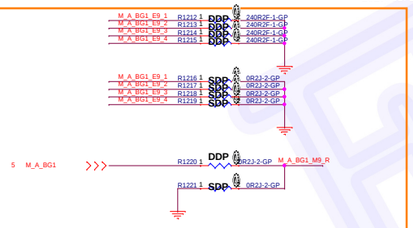






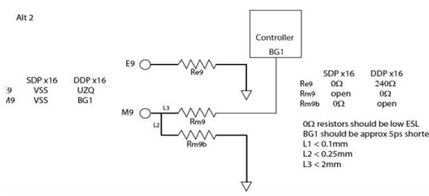


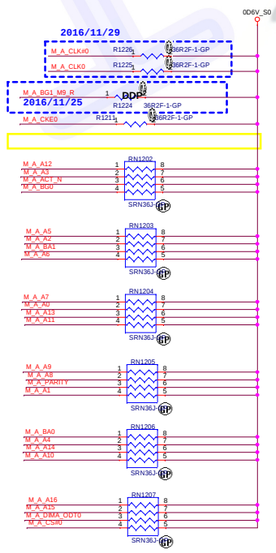
SDP & DDP SETTING

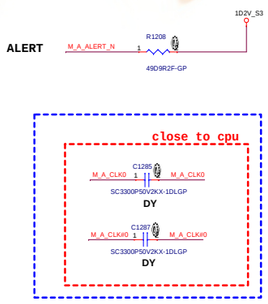


DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little







Eletro-X

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan
Title
DDR3-SODIMM1
Size A1
Document Number
KyloRen 13"
Rev X00
Date: Thursday, June 29, 2017
Sheet of

SSID = MEMORY

Table 4-55. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1µF (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10µF (0603) (All stuffed)	
	VPP	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	5x 10µF (0603)	
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	4x 10µF (0603)	

Table 4-55. DDR4 Memory Down Power Plane Decoupling (Sheet 2 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x16 - 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	64x 1µF (0402) (All stuffed)	
		Distributed around the DRAM devices	20x 10µF (0603) (min of 12 stuffed)	
	VPP	2 as near each x16 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10µF (0603)	
	VTT	2 as near each x16 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	8x 10µF (0603)	

ZZ.00PAD.0Q2

2017/05/10

2016/11/29

2016/11/25

2017/03/07

VDDQ/VDD 1uF x32

VDDQ/VDD 10uF x10

VPP 1uF x16

VPP 10uF x5

VTT 10uF x4

VTT 1uF x16

2017/01/17

SDP & DDP SETTING

DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little

Alt 2

	SDP x16	DDP x16
E9	VSS	UZQ
M9	VSS	BG1
Re9	0Ω	240Ω
Rm9	open	0Ω
Rm9b	0Ω	open

0Ω resistors should be low ESL
BG1 should be approx 5ps shorter
L1 < 0.1mm
L2 < 0.25mm
L3 < 2mm

ALERT

CLK

CTRL/CKE/CMD

close to cpu

2016/11/25 DY

Electro-X

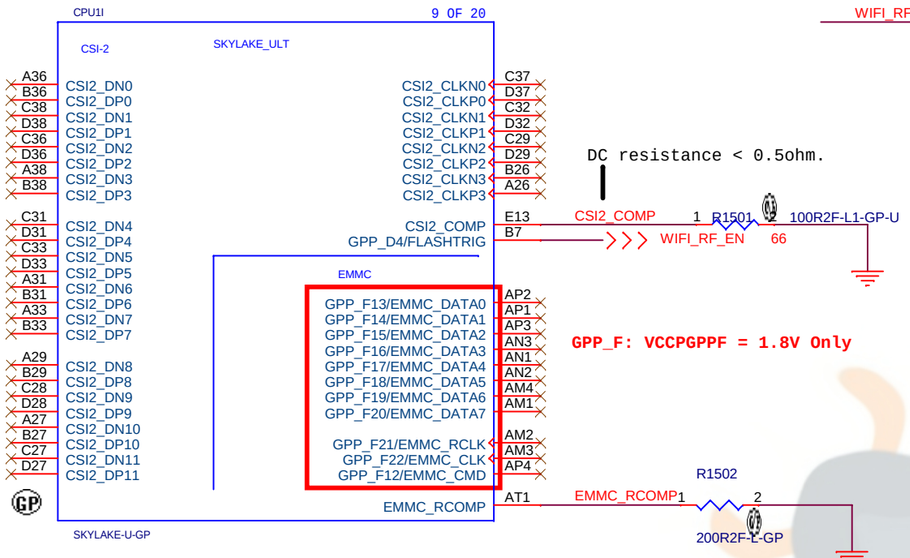
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: A1 | Document Number: KyloRen 13" | Rev: 1.00

Date: Thursday, June 29, 2017 | Sheet: 1 of 1

SSID = PCH



071.SKYLA.000U

DC resistance < 0.5ohm.

CSI2_COMP 1 R1501 2 100R2F-L1-GP-U

WIFI_RF_EN 66

GPP_F: VCCPGPPF = 1.8V Only

EMMC_RCOMP1 R1502 2 200R2F-L-GP

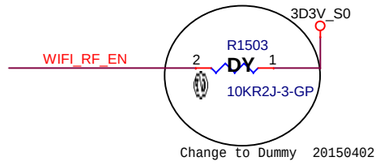


Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(CS-2/EMMC)
Size: A3 | Document Number: KyloRen 13" | Rev: A00
Date: Thursday, June 29, 2017 | Sheet 15 of 106

Eletro-X

SSID= PCH

#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

GPU

LAN

WLAN

HDD1

SSD

Swap Net follow DELL HSIO 20161025

CPU1H — 8 OF 20 — SKYLAKE_ULT — PCIE/USB3/SATA — SSIC / USB3

PCIE1_RXN/USB3_5_RXN
PCIE1_RXP/USB3_5_RXP
PCIE1_TXN/USB3_5_TXN
PCIE1_TXP/USB3_5_TXP
PCIE2_RXN/USB3_6_RXN
PCIE2_RXP/USB3_6_RXP
PCIE2_TXN/USB3_6_TXN
PCIE2_TXP/USB3_6_TXP
PCIE3_RXN
PCIE3_RXP
PCIE3_TXN
PCIE3_TXP
PCIE4_RXN
PCIE4_RXP
PCIE4_TXN
PCIE4_TXP
PCIE5_RXN
PCIE5_RXP
PCIE5_TXN
PCIE5_TXP
PCIE6_RXN
PCIE6_RXP
PCIE6_TXN
PCIE6_TXP
PCIE7_RXN/SATA0_RXN
PCIE7_RXP/SATA0_RXP
PCIE7_TXN/SATA0_TXN
PCIE7_TXP/SATA0_TXP
PCIE8_RXN/SATA1A_RXN
PCIE8_RXP/SATA1A_RXP
PCIE8_TXN/SATA1A_TXN
PCIE8_TXP/SATA1A_TXP
PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP
PCIE10_RXN
PCIE10_RXP
PCIE10_TXN
PCIE10_TXP
PCIE_RCOMPN
PCIE_RCOMPP
PROC_PRDY#
PROC_PREQ#
GPP_A7/PIRQA#
PCIE11_RXN/SATA1B_RXN
PCIE11_RXP/SATA1B_RXP
PCIE11_TXN/SATA1B_TXN
PCIE11_TXP/SATA1B_TXP
PCIE12_RXN/SATA2_RXN
PCIE12_RXP/SATA2_RXP
PCIE12_TXN/SATA2_TXN
PCIE12_TXP/SATA2_TXP

USB3_1_RXN / USB3_1_RXP / USB3_1_TXN / USB3_1_TXP — USB1_USB30_RX_N1 36 / USB1_USB30_RX_P1 36 / USB1_USB30_TX_N1 36 / USB1_USB30_TX_P1 36 — For power share
USB3_2_RXN/SSIC_1_RXN / USB3_2_RXP/SSIC_1_RXP / USB3_2_TXN/SSIC_1_TXN / USB3_2_TXP/SSIC_1_TXP — USB3.0
USB3_3_RXN/SSIC_2_RXN / USB3_3_RXP/SSIC_2_RXN / USB3_3_TXN/SSIC_2_TXN / USB3_3_TXP/SSIC_2_TXP — USB2_USB30_RX_N3 66 / USB2_USB30_RX_P3 66 / USB2_USB30_TX_N3 66 / USB2_USB30_TX_P3 66 — IO board USB3.0
USB3_4_RXN / USB3_4_RXP / USB3_4_TXN / USB3_4_TXP — TYPEC_USB30_RX_N4 38 / TYPEC_USB30_RX_P4 38 / TYPEC_USB30_TX_N4 38 / TYPEC_USB30_TX_P4 38 — Type-c Full
USB2P_1 — USB1_USB20_N 34 / USB1_USB20_P 34 — For power share
USB2P_2 — USB3.0
USB2P_3 — USB2_USB20_N 66 / USB2_USB20_P 66 — IO board USB3.0
USB2P_4 — TYPEC_USB20_N 38 / TYPEC_USB20_P 38 — Type-c Full
USB2P_5 — CCD_USB20_N 55 / CCD_USB20_P 55 — CAMERA
USB2P_6 — CARD1_USB20_N 66 / CARD1_USB20_P 66 — Card Reader
USB2P_7 — BT_USB20_N 66 / BT_USB20_P 66 — WLAN (BT)
USB2P_8 — Touch Panel
USB2P_9 — FP1_USB20_N 92 / FP1_USB20_P 92 — Fingerprint Reader
USB2P_10 — DC resistance < 0.5ohm. — Remove Sensor HUB
USB2_COMP — USBCOMP 1 R1603 113R2F-GP
USB2_IC — USB2_ID
USB2_VBUSSENSE — USB2_VBUSSENSE
GPP_E9/USB2_OC0# — USB_OC0# 34,35
GPP_E10/USB2_OC1# — USB_OC1# 66
GPP_E11/USB2_OC2# — USB_OC2#
GPP_E12/USB2_OC3# — USB_OC3#
GPP_E4/DEVSLP0 — SSD_DEVSLP 63
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2
GPP_E0/SATAXPCIE0/SATAGP0 — GPP_E0/SATAXPCIE0/SATAGP0 1 TP1602 TPAD14-OP-GP
GPP_E1/SATAXPCIE1/SATAGP1 — GPP_E1/SATAXPCIE1/SATAGP1 1 TP1603 TPAD14-OP-GP
GPP_E2/SATAXPCIE2/SATAGP2 — M2_SSD_PEDET 63
GPP_E8/SATALED# — SATA_LED# 64

SIO_EXT_SC# — 3D3V_S0 — R1608 2 1 10KR2J-3-GP

(#543016) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

3D3V_SS_PCH — RN1601 — USB_OC2# 8 2 / USB_OC3# 7 3 / USB_OC4# 6 4 / USB_OC1# 5 1 — SRN10KJ-6-GP

USB2_ID — R1601 2 0R0402-PAD 1
USB2_VBUSSENSE — R1602 2 0R0402-PAD 1
2016/12/28

Follow SKL PDG design guide

3D3V_S0 — R1606 2 1 10KR2J-3-GP — SATA_LED#

(#543611)
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

(#543016) Unused SATAGP[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 KΩ to 10 KΩ on the motherboard.
Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

Swap Net follow DELL HSIO 20161025

SCD1U25V2KX-1-DL-GP — WLAN_PCIE_TX_N_C / WLAN_PCIE_TX_P_C — C1601 1 1 C1602

63 MSATA_PCIE_RX_N9 / MSATA_PCIE_RX_P9 / MSATA_PCIE_TX_N9 / MSATA_PCIE_TX_P9
63 MSATA_PCIE_RX_N10 / MSATA_PCIE_RX_P10 / MSATA_PCIE_TX_N10 / MSATA_PCIE_TX_P10
R1604 1 — 10MR2F-L1-GP-U — PCIE_RCOMPN / PCIE_RCOMPP
99 XDP_PRDY# / 99 XDP_PREQ#
63 MSATA_PCIE_RX_N11 / MSATA_PCIE_RX_P11 / MSATA_PCIE_TX_N11 / MSATA_PCIE_TX_P11
63 MSATA_SATA_RX_N2 / MSATA_SATA_RX_P2 / MSATA_SATA_TX_N2 / MSATA_SATA_TX_P2

071.SKYLA.000U

+V1.8A_SP — R1607 1 2 10KR2J-3-GP — PIRQA#

Layout Note:
1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

USB 2.0 Table

Pair	Device
1	USB3.0 port1
2	N/A
3	USB3.0 Port2 (IOBD)
4	Type-c
5	CAMERA
6	WLAN
7	Touch Panel
8	Card Reader

#545659 (SKL_PCH_U_Y_EDS Rev0.7)

Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

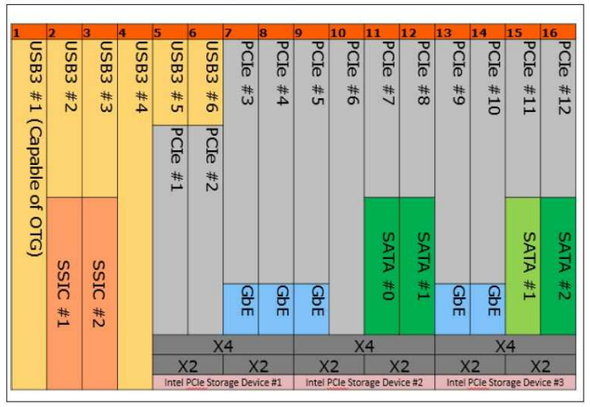


Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

Eletro-X

<Core Design>
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU (PCIE/SATA/USB)
Size: A1 | Document Number: KyloRen 13" | Rev: 1.00
Date: Thursday, June 29, 2017 | Sheet

SSID = PCH

R1709,R1723,R1703,R1724 merge to RN1704

3D3V_S5 — RN1704 — AC_PRESENT, PCIE_WAKE#_CPU, PCH_BATLOW#, GPD11/LANPHYPC — SRN10KJ-6-GP

SPD11 pull high by Intel PDG1.3 request

3D3V_S5 — R1711 0R0603-PAD — +VCCPDSW_3P3

Layout note: 3 PAD SHARING

RTC_AUX_S5 — R1730 330KR2J-L1-GP — SM_INTRUDER#

#544669 (CRB): 330k.

+V3.3A_SIP — R1731 20KR2J-L2-GP — EXT_PWR_GATE#

[#543016 Rev0.7]
EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k pull-down that is active during the early portion of the power up sequence

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.

H_CPUPWRGD — R1714 10KR2J-3-GP DY — EC1701 AZ5725-01FDR7G-GP DY — EMI DVT1 0210

2016/12/29

RN1703 — PM_RSMRST#, PM_PCH_PWROK — SRN10KJ-5-GP

R1717 DY 10KR2J-3-GP — SYS_PWROK

+V1.8A_SIP — R1738 DY 10KR2J-3-GP — ME_SUS_PWR_ACK_R

ME_SUS_PWR_ACK_R — R1708 0R0402-PAD — SUSACK#_R

2016/12/28

AOZ Power switch, P/N: 074.01334.0093
Low Rds(on)= 5m Ohm
Turn on rise time = 10us

+V3.3A_SIP — R1701 10KR2J-3-GP

99 XDP_DBRESET# — PCH_PLTRST#

TPAD14-OP-GP P1705 — H_CPUPWRGD, H_VCCST_PWRGD

SYS_PWROK, PM_PCH_PWROK, PCH_DPWROK

24,99 SYS_PWROK
24,26 RESET_OUT# — PM_RSMRST# — R1706 0R0402-PAD, R1704 0R0402-PAD

2016/12/28

ME_SUS_PWR_ACK_R, SUSACK#_R

2017/04/24

24 PCIE_WAKE#_CPU — +VCCPDSW_3P3 — R1707 10KR2J-3-GP — LAN_WAKE#

GPD11/LANPHYPC

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

CPU1K — 11 OF 20 — SYSTEM POWER MANAGEMENT — SKYLAKE_ULT

GPP_B13/PLTRST#, SYS_RESET#, RSMRST#, PROCPWRGD, VCCST_PWRGD, SYS_PWROK, PCH_PWROK, DSW_PWROK, GPP_A13/SUSWARN#/SUSPWRDNACK, GPP_A15/SUSACK#, WAKE#, GPD2/LAN_WAKE#, GPD11/LANPHYPC, GPD7/USB2_WAKEOUT#

GPP_B12/SLP_S0#, GPD4/SLP_S3#, GPD5/SLP_S4#, GPD10/SLP_S5#, SLP_SUS#, SLP_LAN#, GPD9/SLP_WLAN#, GPD6/SLP_A#, GPD3/PWRBTN#, GPD1/ACPRESENT, GPD0/BATLOW#, GPP_A11/PME#/INTRUDER#, GPP_B11/EXT_PWR_GATE#, GPP_B2/VRALERT#

SKYLAKE-U-GP

071.SKYLA.000U

SIO_SLP_S0# 24,40,91
SIO_SLP_S3# 24,40,51
SIO_SLP_S4# 40,54
AUX_EN_WOWL 24,61
SIO_PWRBTN# 24,99
AC_PRESENT
PCH_BATLOW#
SM_INTRUDER#
EXT_PWR_GATE#
VRALERT# — TP1708 TPAD14-OP-GP

BATLOW#:
Pull-up required even if not implemented.

AC_PRESENT — EC1707 SCD1U16V2KX-3GP DY

Dis-wire with XDP_PM_RSMRST_PWRGD_XDP

24,40 RUNPWROK

2017/03/16

3D3V_S0 — R1718 100KR2F-L1-GP — H_VCCST_PWRGD — CT211 SCD1U25V2KX-1-DL-GP DY — EC1708 AZ5725-01FDR7G-GP DY — EMI DVT1 0210

R1716 100KR2F-L1-GP DY — EC1709 AZ5725-01FDR7G-GP DY — EMI DVT1 0210

R1719 47KR2F-GP

2016/12/07 for power sequence

R1722 & EC1708 modify to 100k and 0.01uF at DVT1

26,63,66,91,99 PLT_RST# — R1713 0R0402-PAD — PCH_PLTRST#

R1715 100KR2J-1-GP DY — C1701 SC220P50V2KX-3GP DY

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

+VCCMPHYGTAON_1P0
SKL: 1.0V
+VCCMPHYGTAON_1P0(ICCMAX.=3.5A)

1D0V_S5 — EC1710 SCD2D2U03V2KX-DL-GP DY — R1724 0R0805-PAD, R1735 0R0805-PAD

2017/05/08

+VCCMPHYGTAON_1P0_LS_SIP — C1704 SC10U6D3V3MX-DL-GP

RF request 2016/01/12 modify

Follow Iris SKL 2015/11/30 modify

XDP_DBRESET#, SYS_PWROK, PLT_RST#, RESET_OUT#, 3V_5V_POK — ED1701 AZ5125-02S-R7G-GP — EC1706 SC1KP50V2KX-1GP DY — EC1704 AZ5725-01FDR7G-GP DY — EC1705 AZ5725-01FDR7G-GP DY

75.05125.07D

2017/05/05

4th = 84.DMN66.03F
3rd = 75.00601.07C
2nd = 84.2N702.E3F
84.2N702.A3F

D1701 RB751V-40H-GP — ACOK_IN_M 43,44

83.R2004.G8F

Q1702 2N7002KDW-GP

3D3V_AUX_S5 — R1737 100KR2J-1-GP — PM_RSMRST#_M

NON DS3

PM_RSMRST# — R1720 0R0402-PAD — PM_RSMRST#

2016/12/28

Reserve by NON DS3 function 20150413

3D3V_AUX_S5 — R1727 100KR2J-1-GP — NON DS3

R1726 10KR2J-3-GP

Q1701 PJT138KA-GP

3V_5V_POK# — PM_RSMRST# — 1KR2J-1-GP R1702 — R1728 0R0402-PAD

2016/12/28

3V_5V_POK — PCH_RSMRST# 24,99

C1710 SCD47U10V2KX-GP DY — EC1712 SCD1U16V2KX-3GP DY

Dummy C1710 by it's useless

075.00138.0A7C

2017/03/09

EC1711 modify to 100k and 0.01uF at DVT1 20150203

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)
Size: A2 | Document Number: KyloRen 13" | Rev: A00
Date: Thursday, June 29, 2017 | Sheet 17 of 58

Eletro-X

SSID = PCH

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PCH Prim

3D3V_S5_PCH — R1824 1KR2J-1-GP (DY) — SPI_SI_CPU — R1825 1KR2J-1-GP (DY)

R1835 and R1834 merge to RN1802
2015/10/06 modify

3D3V_S5_PCH — RN1802 SRN1KJ-7-GP — SPI_HOLD_ROM, SPI_WP_ROM

PLACE WITHIN 1.1 INCH OF PCH

99 SPI_SI_XDP — R9935 XDP 1KR2J-1-GP — SPI_SI_CPU (#543016)Optional, can be left as OPEN/No-Connect.

3D3V_S5_PCH — RN1807 SRN2K2J-4-GP — SML1_SMBDATA, SML1_SMBCLK, SML0_SMBDATA, SML0_SMBCLK

DVT1 0210, Reserve by Intel MOW

SML1ALERT# — 150KR2J-GP — R1837

SMB_ALERT# — R1836 2K2R2J-2-GP

SRN2K2J-1-GP — MEM_SMBCLK, MEM_SMBDATA — RN1811

For eSPI

24,68 ESPI_IO[3..0] — RN1806 SRN15J-GP — ESPI_IO3, ESPI_IO1, ESPI_IO2, ESPI_IO0 — PCH_ESPI_IO3, PCH_ESPI_IO1, PCH_ESPI_IO2, PCH_ESPI_IO0

R1806,R1807,R1808,R1809 merge to RN1803
2015/10/06 modify

+V1.8A_SIP — R1820 10KR2J-3-GP — SIO_RCIN# — R1821 10KR2J-3-GP — ESPI_ALERT#

SERIRQ PH:
PDG: 8.2k
CRB: 10k

RN1803 SRN10J-1-GP

25,91 SPI_CLK_ROM — SPI_CLK_CPU
25,91 SPI_SO_ROM — SPI_SO_CPU
25,91 SPI_SI_ROM — SPI_SI_CPU
25,99 SPI_WP_ROM — SPI_WP_CPU
25 SPI_HOLD_ROM — 10R2F-L-GP — R1811 — SPI_HOLD_CPU
25 SPI_CS_ROM_N0 — 0R0402-PAD — R1812 — SPI_CS_CPU_N0
91 SPI_CS_ROM_N2 — 0R2J-2-GP — R1838 — SPI_CS_CPU_N2

2016/11/25 change to CS2

2017/05/08

70 FFS_INT1 — 91 TPM_SPI_IRQ# — TPM

CPU1E — 5 OF 20

SPI - FLASH: SPI0_CLK (AV2), SPI0_MISO (AW3), SPI0_MOSI (AV3), SPI0_IO2 (AW2), SPI0_IO3 (AU4), SPI0_CS0# (AU3), SPI0_CS1# (AU2), SPI0_CS2# (AU1)

Strap

SPI - TOUCH: GPP_D1/SPI1_CLK (M2), GPP_D2/SPI1_MISO (M3), GPP_D3/SPI1_MOSI (J4), GPP_D21/SPI1_IO2 (V1), GPP_D22/SPI1_IO3 (V2), GPP_D0/SPI1_CS# (M1)

TPAD14-OP-GP TP1804 — CPU_D4_TP
TPAD14-OP-GP TP1805 — CPU_D5_TP
TPAD14-OP-GP TP1806 — CPU_D6_TP

C LINK: CL_CLK (G3), CL_DATA (G2), CL_RST# (G1)

SKYLAKE_ULT

SMBUS, SMLINK: GPP_C0/SMBCLK (R7) MEM_SMBCLK; GPP_C1/SMBDATA (R8) MEM_SMBDATA; GPP_C2/SMBALERT# (R10) SMB_ALERT#; GPP_C3/SML0CLK (R9) SML0_SMBCLK; GPP_C4/SML0DATA (W2) SML0_SMBDATA; GPP_C5/SML0ALERT# (W1) SML0_ALERT#; GPP_C6/SML1CLK (W3) SML1_SMBCLK; GPP_C7/SML1DATA (V3) SML1_SMBDATA; GPP_B23/SML1ALERT#/PCHHOT# (AM7) SML1ALERT#

SML1_SMBCLK, SML1_SMBDATA — 24,26

LPC: GPP_A1/LAD0/ESPI_IO0 (AY13) PCH_ESPI_IO0; GPP_A2/LAD1/ESPI_IO1 (BA13) PCH_ESPI_IO1; GPP_A3/LAD2/ESPI_IO2 (BB13) PCH_ESPI_IO2; GPP_A4/LAD3/ESPI_IO3 (AY12) PCH_ESPI_IO3; GPP_A5/LFRAME#/ESPI_CS# (BA12); GPP_A14/SUS_STAT#/ESPI_RESET# (BA11); GPP_A9/CLKOUT_LPC0/ESPI_CLK (AW9) PCH_ESPI_CLK; GPP_A10/CLKOUT_LPC1 (AY9); GPP_A8/CLKRUN# (AW11)

ESPI_CS# — 24,68
ESPI_RESET# — 24,68
CLKRUN# — 24

GPP_A0/RCIN# (AW13) — SIO_RCIN#
GPP_A6/SERIRQ (AY11) — 24 ESPI_ALERT#

RCIN#:
Frequency to Avoid: 33 MHz

2016/11/4

SKYLAKE-U-GP — 20160820 DAIVD

071.SKYLA.000U

PCH_ESPI_CLK — R1805 15R2F-2-GP — ESPI_CLK 24,68

DY — EC1801 SC1U25V2ZN-4GP — ECI3501

3D3V_S0 — RN1810 SRN10KJ-5-GP — 3D3V_S0

2N7002KDW-GP — Q1801

MEM_SMBDATA — PCH_SMBDATA 99

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

PCH_SMBCLK 99

MEM_SMBCLK

For eSPI

Table 9-1. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
GSPI1_MOSI/ GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal Pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). Bit 6: 0 = SPI (Default); 1 = LPC Notes: 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
SML0ALERT#/ GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This Signal has a weak internal Pull-down. 0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC. Notes: 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

3D3V_S5_PCH — R1822 1KR2J-1-GP — SML0_ALERT# — R1823 1KR2J-1-GP (DY)

Table 3: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash

ESPI Enable Strap (ESPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BBS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-up. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-up.

2016/10/31modify

RTC_X1 — R1815 10MR2J-L-GP — RTC_X2

X1802 — C1804 SC1P50V2CN-3-GP — C1803 SC1P50V2CN-3-GP — XTAL-32D768KHZ-6PF-GP — 82.30001.G01

2017/03/15 2017/03/15

2016/12/14 vendor suggest

R1839 0R0402-PAD-2-GP — XTAL24_IN_R

X1801 — U22 INPUT/OUTPUT#1, NC#2, INPUT/OUTPUT#3 — XTAL-24MHZ-135-GP — 082.30006.0041

C1801 SC18P50V2JN-1DLGP — U22

2017/05/09

R1802 1MR2J-1-GP — U22

R1840 0R0402-PAD-2-GP — XTAL24_OUT_L

R1810 0R0402-PAD — XTAL24_OUT_R

C1802 SC18P50V2JN-1DLGP — U22

3D3V_S0 — RN1813 SRN10KJ-6-GP — CLK_PCIE_NVME_REQ#, CLK_PCIE_SD_REQ#, CLK_PCIE_TBT_REQ#, CLK_PCIE_WLAN_REQ#

2017/04/24 2016/11/04

CPU1J — 10 OF 20 — CLOCK SIGNALS — SKYLAKE_ULT

GPU: 66 WLAN_CLK_CPU# — CLKOUT_PCIE_N0 (D42), CLKOUT_PCIE_P0 (C42), GPP_B5/SRCCLKREQ0# (AR10)

WLAN: 66 WLAN_CLK_CPU — CLKOUT_PCIE_N1 (B42), CLKOUT_PCIE_P1 (A42), GPP_B6/SRCCLKREQ1# (AT7)
66 CLK_PCIE_WLAN_REQ# — 2016/11/04

LAN: CLKOUT_PCIE_N2 (D41), CLKOUT_PCIE_P2 (C41), GPP_B7/SRCCLKREQ2# (AT8)

2016/11/04

2017/04/24 CLK_PCIE_SD_REQ# — CLKOUT_PCIE_N3 (D40), CLKOUT_PCIE_P3 (C40), GPP_B8/SRCCLKREQ3# (AT10)

SSD: 63 MSATA_CLK_CPU# — CLKOUT_PCIE_N4 (B40), CLKOUT_PCIE_P4 (A40), GPP_B9/SRCCLKREQ4# (AU8)
63 MSATA_CLK_CPU
63 CLK_PCIE_NVME_REQ#

2017/04/24 CLK_PCIE_TBT_REQ# — CLKOUT_PCIE_N5 (E40), CLKOUT_PCIE_P5 (E38), GPP_B10/SRCCLKREQ5# (AU7)

SKYLAKE-U-GP

071.SKYLA.000U

CLKOUT_ITPXDP# (F43) — PCIE_CLK_XDP_N 99
CLKOUT_ITPXDP_P (E43) — PCIE_CLK_XDP_P 99

GPD8/SUSCLK (BA17) SUSCLK_R — R1813 0R0402-PAD — SUS_CLK 24

XTAL24_IN (E37)
XTAL24_OUT (E35)

XCLK_BIASREF (E42) — R1803 2K7R2F-GP — +V1.00A_SIP — +V1.05S_AXCK_LCPLL
Intel recommend: 2.71k ohm 1%

RTCX1 (AM18) RTC_X1
RTCX2 (AM20) RTC_X2

SRTCRST# (AN18) SRTC_RST#
RTCRST# (AM16) RTC_RST#

24 RTCRST_ON — Q1802 2N7002K-2-GP — R1816 10KR2J-3-GP

84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31

RTC_AUX_S5 — RN1801 SRN20KJ-1-GP — SUSCLK_R — SRTC_RST# — RTC_RST#

DY — EC1803 SC4D7P50V2BN-GP

G1801 GAP-0-PCB-GP — C1805 SC1U10V2KX-1DLGP — C1806 SC1U10V2KX-1DLGP

ED1801 DY — ED1802 DY — PESD5V0U1BL-GP-U1

20160816 EMI

(#514849)

Layout: Place at the open door area.

2017/03/17

+V1.8A_SIP — R1818 8K2R2F-1-GP (DY) — CLKRUN#

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPC/SPI/SMBUS/CLOCK)

Size: A2 | Document Number: KyloRen 13" | Rev: A00

Date: Thursday, June 29, 2017 | Sheet 18 of 106

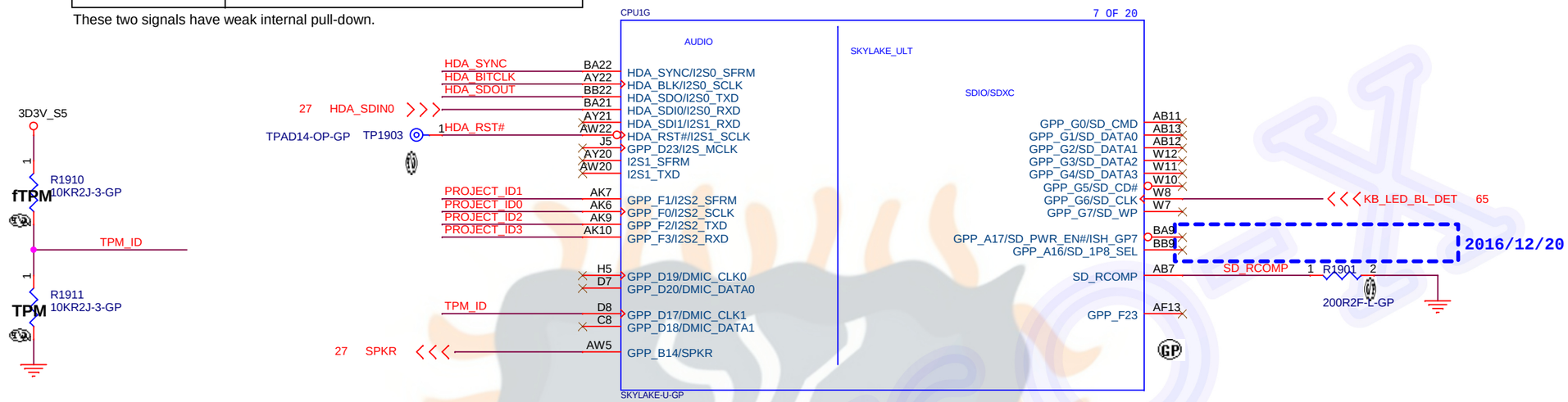
Eletro-X

SSID = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.



PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default High = Enable *

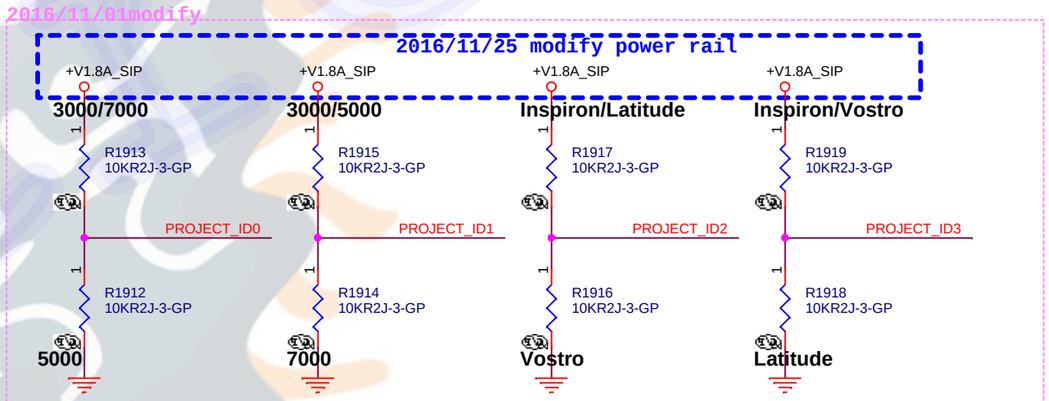
The internal pull-down is disabled after PLTRST# deasserts

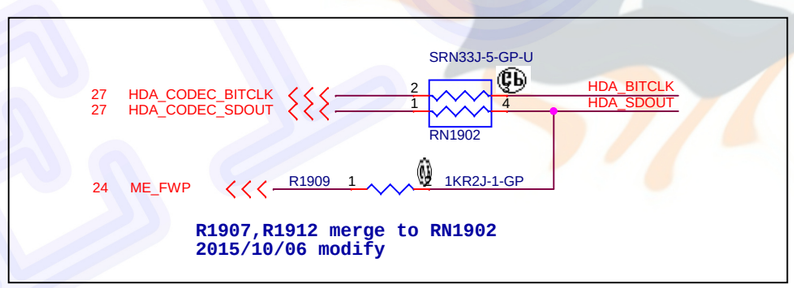
PCH strap pin:

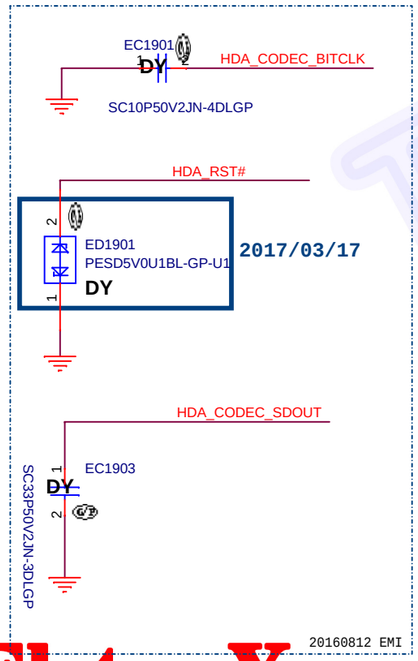
NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts

071.SKYLA.000U







Eletro-X

<Core Design>

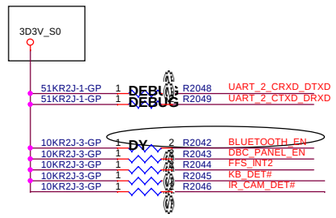
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

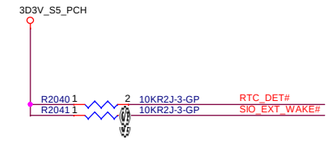
Title: CPU (AUDIO/SDIO/SDXC)

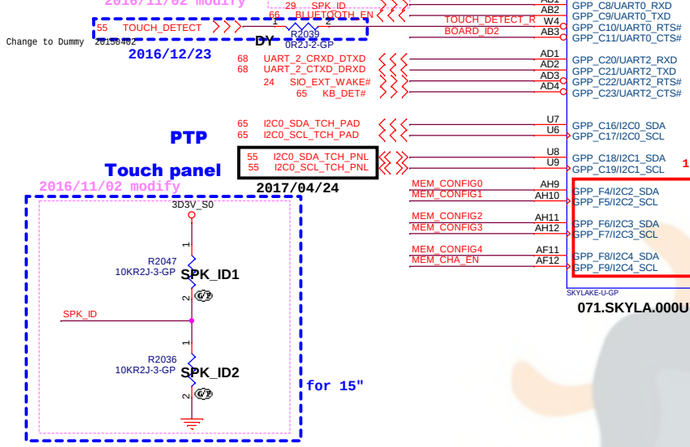
Size: A3 | Document Number: KyloRen 13" | Rev: A00

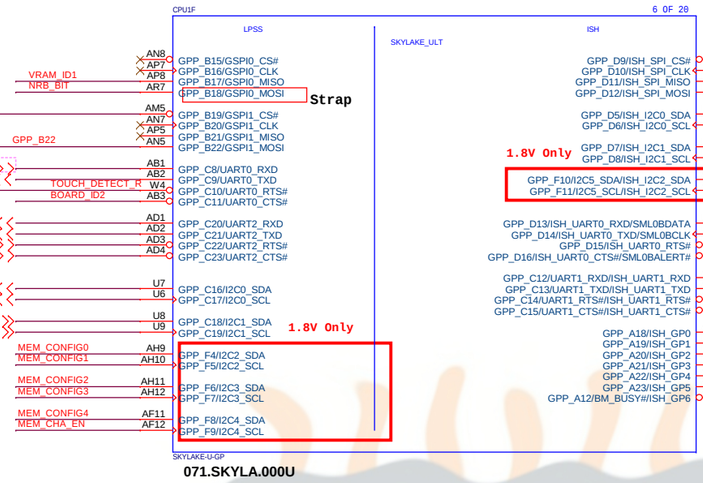
Date: Thursday, June 29, 2017 | Sheet 19 of 106

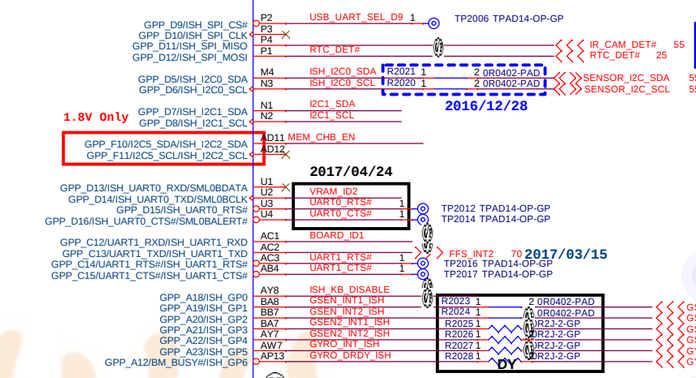
SSID = PCH

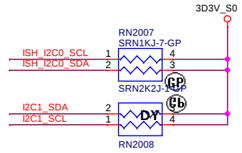




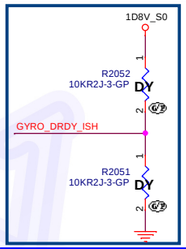




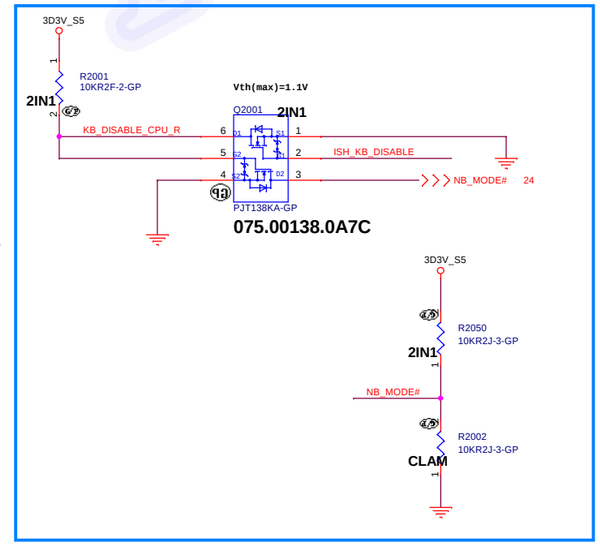




(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

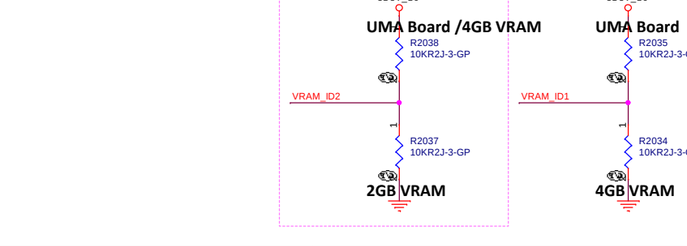


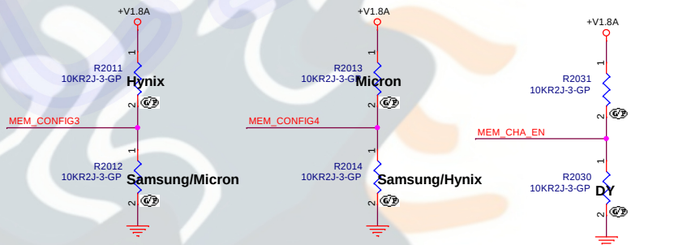
(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.



RAM ID

Vender	MEM_CONFIG [0]	MEM_CONFIG[1:2]	MEM_CONFIG[3:4]	Mfr. PN	Wistron. P/N	Capacity
Samsung	0	01	00	K4AAG165WB-BCRC	TBD	16G
Hynix	0	01	10	H5ANAG6NAMR-UHC	TBD	16G
Micron	0	01	01	MT40A1G16WBU-083E	072.40116.0B0U	16G
Samsung	1	10	00	K4A8G165WB-BCRC	TBD	8G
Hynix	1	10	10	H5AN8G6NAFR-UHC	TBD	8G
Micron	1	10	01	MT40A512M16JY-083E	072.40512.0B0U	8G
Samsung	1	00	00	K4A4G165WE-BCRC	072.44165.0B0U	4G
Hynix	1	00	10	H5AN4G6NBJR-UHC*	TBD	4G
Micron	1	00	01	MT40A256M16GE-083E	072.40256.0A0U	4G

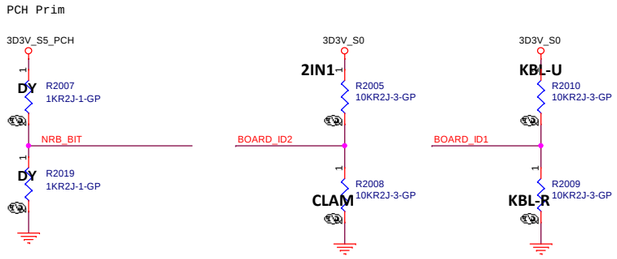




PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (LPSS/ISH)
Size: A2 | Document Number: KyloRen 13" | Rev: A00
Date: Thursday, June 29, 2017 | Sheet 20 of 56

Eletro-X

SSID = PCH

For eSPI

+V1.8A_SIP

+V1.00A_SIP

+V3.3A_SIP

CPU1O

15 OF 20

CPU POWER 4 OF 4

SKYLAKE_ULT

+VCCPRIM_CORE

2.57A

1.8V Only

EC2101 SCD1U25V2KX-1-DL-GP

C2120 SCD1U10V2KX-1DLGP

DY

+VCCDSW_1P0

+V1.00A_SIP

+VCCMPHYGTAON_1P0_LS_SIP

+VCCAMPHYPLL_1P0

+VCCAPLL_1P0

+V1.00A_SIP

+VCCPDSW_3P3

+V3.3A_SIP

R2101 1 2 0R0402-PAD

+VCCPAZIO

+V3.3A_SIP

+VCCMPHYGTAON_1P0_LS_SIP

+V3.3A_SIP

+V1.00A_SIP

+VCCMPHYGTAON_1P0_LS_SIP

AB19	VCCPRIM_1P0
AB20	VCCPRIM_1P0
P18	VCCPRIM_1P0
AF18	VCCPRIM_CORE
AF19	VCCPRIM_CORE
V20	VCCPRIM_CORE
V21	VCCPRIM_CORE
AL1	DCPDSW_1P0
K17	VCCMPHYAON_1P0
L1	VCCMPHYAON_1P0
N15	VCCMPHYGT_1P0_N15
N16	VCCMPHYGT_1P0_N16
N17	VCCMPHYGT_1P0_N17
P15	VCCMPHYGT_1P0_P15
P16	VCCMPHYGT_1P0_P16
K15	VCCAMPHYPLL_1P0
L15	VCCAMPHYPLL_1P0
V15	VCCAPLL_1P0
AB17	VCCPRIM_1P0_AB17
Y18	VCCPRIM_1P0_Y18
AD17	VCCDSW_3P3_AD17
AD18	VCCDSW_3P3_AD18
AJ17	VCCDSW_3P3_AJ17
AJ19	VCCHDA
AJ16	VCCSPI
AF20	VCCSRAM_1P0
AF21	VCCSRAM_1P0
T19	VCCSRAM_1P0
T20	VCCSRAM_1P0
AJ21	VCCPRIM_3P3_AJ21
AK20	VCCPRIM_1P0_AK20
N18	VCCAPLLEBB

AK15	VCCPGPPA
AG15	VCCPGPPB
Y16	VCCPGPPC
Y15	VCCPGPPD
Y16	VCCPGPPE
AF16	VCCPGPPF
AD15	VCCPGPPG
V19	VCCPRIM_3P3_V19
T1	VCCPRIM_1P0_T1
AA1	VCCATS_1P8
AK17	VCCRTCPRIM_3P3
AK19	VCCRTC_AK19
BB14	VCCRTC_BB14
BB10	DCPRTC
A14	VCCCLK1
K19	VCCCLK2
L21	VCCCLK3
N20	VCCCLK4
L19	VCCCLK5
A10	VCCCLK6
AN11	GPP_B0/CORE_VID0
AN13	GPP_B1/CORE_VID1

+V1.8A_SIP

+V3.3A_SIP

+VCCPRTC_3P3

VCCRTCEXT C2112 1 SCD1U25V2KX-1-DL-GP

+V1.00A_SIP

+VCCCLK2

+V1.00A_SIP

+VCCCLK4

+V1.00A_SIP

+VCCCLK5

V0.85A_VID0 1 TP2101 TPAD14-OP-GP

V0.85A_VID1 1 TP2102 TPAD14-OP-GP

071.SKYLA.000U

SKYLAKE-U-GP

+VCCPRTC_3P3

C2118 SCD1U25V2KX-1-DL-GP

C2117 SCD1U10V2KX-1DLGP

Layout Note:

0.1uF:
C2118 near AK19
1uF:
C2117 near Ak19

RTC_AUX_S5 — R2106 — +VCCPRTC_3P3 — 0R0603-PAD

+VCCMPHYGTAON_1P0_LS_SIP — R2107 — +VCCAMPHYPLL_1P0 — 0R0603-PAD

+V1.00A_SIP — R2108 — +VCCAPLL_1P0 — 0R0603-PAD

+V1.00A_SIP — R2109 — +VCCCLK2 — 0R0603-PAD

+V1.00A_SIP — R2110 — +VCCCLK4 — 0R0603-PAD

+V1.00A_SIP — R2111 — +VCCCLK5 — 0R0603-PAD

DELETE, 20160810 Nick

+V3.3A_SIP

C2105 C2106 C2107 C2109 C2110 SCD1U10V2KX-1DLGP

C2111 SCD1U25V2KX-1-DL-GP

Layout Note:

1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19

+V1.8A_SIP +VCCPRIM_CORE +VCCDSW_1P0

C2108 C2102 C2103 SCD1U10V2KX-1DLGP

DY

Layout Note:

22uF:
C2113 near K15

+V1.00A_SIP

C2101 C2104 C2121 SCD1U10V2KX-1DLGP

Layout Note:

1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2121 near AL1

+VCCAMPHYPLL_1P0

C2113 SCC22U6D3V3MX-1-GP

DY

+VCCAPLL_1P0

C2114 SCC22U6D3V3MX-1-GP

DY

Layout Note:

22uF:
C2113 near K15

+V1.00A_SIP +VCCCLK2 +VCCCLK4 +VCCCLK5

C2116 C2117 C2119 C2122 SCC22U6D3V3MX-1-GP

Layout Note:

1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

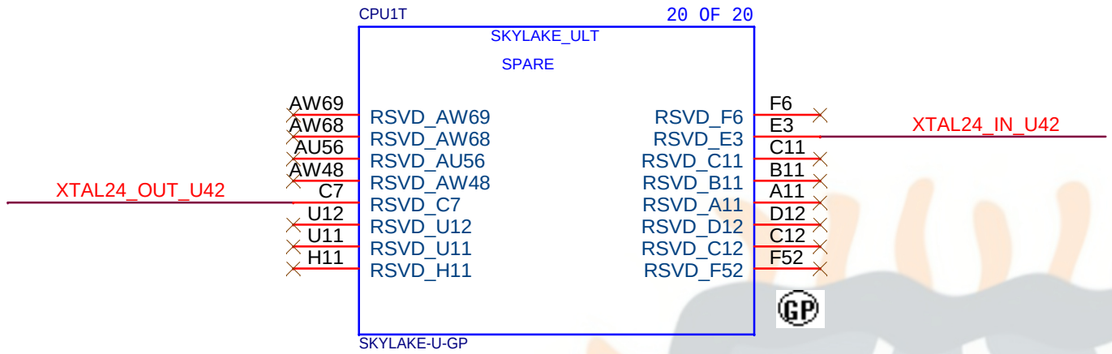
Title: CPU (POWER1)

Size: A2 | Document Number: KyloRen 13" | Rev: A00

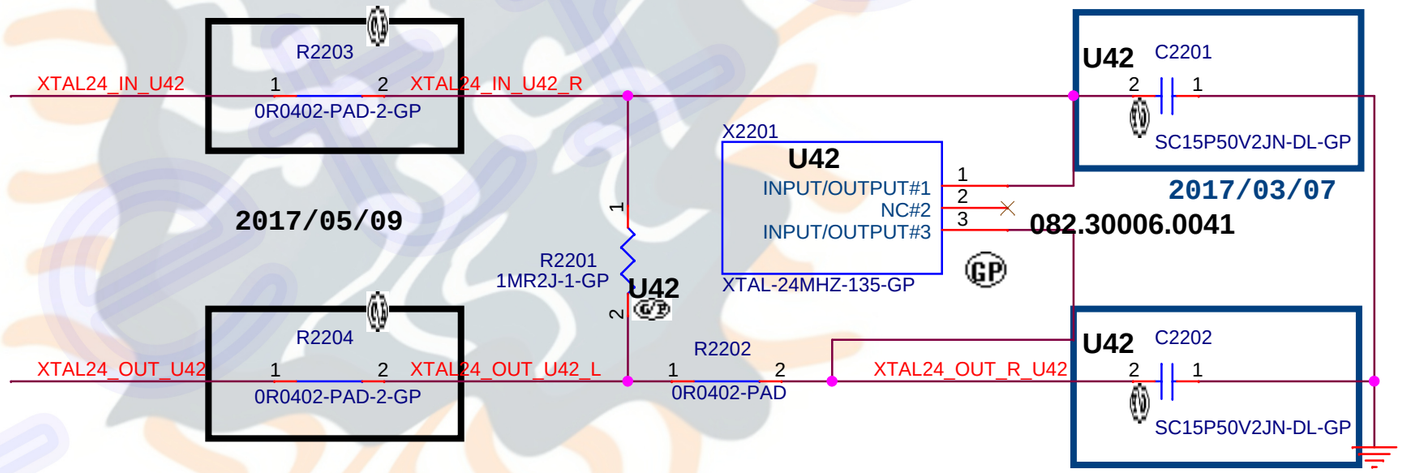
Date: Thursday, June 29, 2017 | Sheet 21 of 56

Eletro-X

SSID = PCH



071.SKYLA.000U



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

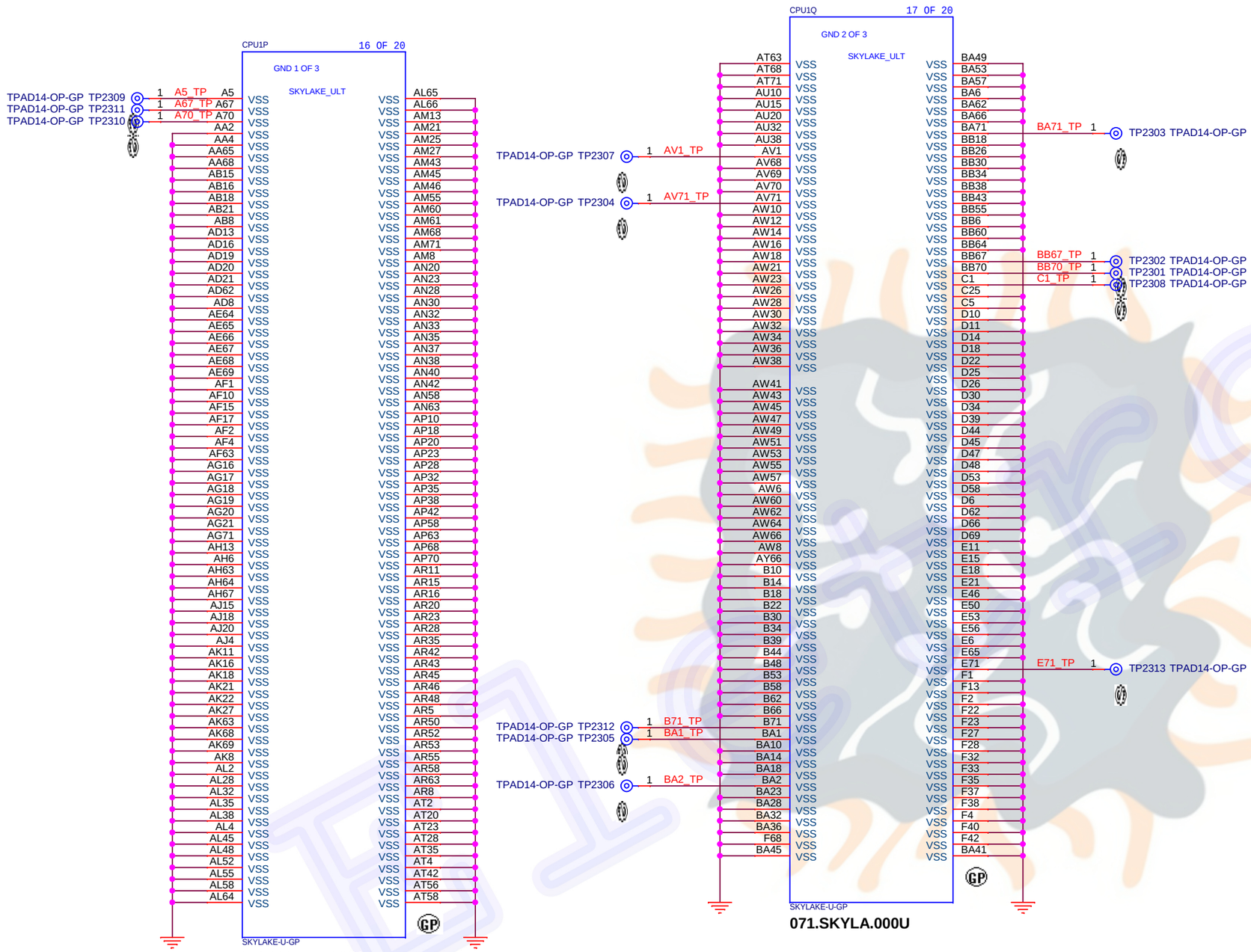
Title: *CPU_(RSVD)*

Size: A4 | Document Number: *KyloRen 13"* | Rev: *A00*

Date: Thursday, June 29, 2017 | Sheet 22 of 106

Eletro-X

SSID = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(VSS)
Size: A3 | Document Number: KyloRen 13" | Rev: A00
Date: Thursday, June 29, 2017 | Sheet 23 of 106

Eletro-X

SSID = KBC

Just for Starload placement
2015/09/23 modify

Layout Note:
Need very close to EC

2017/05/08

2017/03/21

Just for Starload placement
2015/09/23 modify

If don't need RTC alarm wake up, can change to 3D3V_AUX_S5

For eSPI

2016/11/08modify

BOARD_ID VERSION A/D	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
KyloRen_X00	100.0K	10.0K	3.0V
KyloRen_X01	100.0K	17.8K	2.801V
KyloRen_X02	100.0K	27.0K	2.598V
KyloRen_X03	100.0K	37.4K	2.402V
KyloRen_X04	100.0K	49.9K	2.201V
KyloRen_X05	100.0K	64.9K	2.001V
KyloRen_A00	100.0K	82.5K	1.808V
KyloRen_A01	100.0K	107K	1.594V
KyloRen_A02	100.0K	154K	1.299V
KyloRen_A03	100.0K	200KK	1.100V

TBD_20160518

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
TBD	100.0K	10.0K(64.10025.6DL)	3.0V
KyloRen 13" UMA Clamshell	100.0K	17.8K()	2.801V
KyloRen 13" UMA 2in1	100.0K	27.0K()	2.598V
TBD	100.0K	37.4K()	2.402V
KyloRen 15" UMA Clamshell	100.0K	49.9K()	2.201V
KyloRen 15" UMA 2in1	100.0K	64.9K()	2.001V
TBD	100.0K	82.5K()	1.808V
KyloRen 15" DIS Clamshell	100.0K	107K()	1.594V
KyloRen 15" DIS 2in1	100.0K	154K()	1.299V
	100.0K	200K()	1.100V

2016/11/07modify

CPU/ Thermal
For CCG4/I2C/USB Mux

BATTER /CHARGER

Change symbol part number, because origin symbol is DELL OBS part
83.R2004.G8F

2016/12/06 follow 15"

Need very close to EC, PDG: <0.5 inches.

2016/12/28

2017/03/09

Q2412 and Q2413 merge
24014/12/23 modify
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

2016/12/13
2016/12/23
2016/12/22

2017/01/24
2017/03/14

Nick 2016/05/16 modify

Reserve resistor, 20141118

2016/12/22

RUNPWROK assert,
delay 10ms; PCH_PWROK assert.

Microchip: Use CL=9p Xtal - C = 10p

2016/12/22

Layout Note:
Connect GND and AGND planes via either
0R resistor or connect directly.

2016/12/28 modify follow 15"

2016/12/29

2017/03/07

2017/03/14

2017/05/08

Change symbol part number, because origin symbol is DELL OBS part 20150116 2040

For Typec charge detect modify 2017/05/10

Reserve by NON DS3 function 20150413

For eSPI

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

2015/09/22 modify

2017/03/17

Just for Starload placement
2015/09/23 modify

Power Switch Logic(PSL)

2016/12/20 modify

2017/05/15

<Core Design>

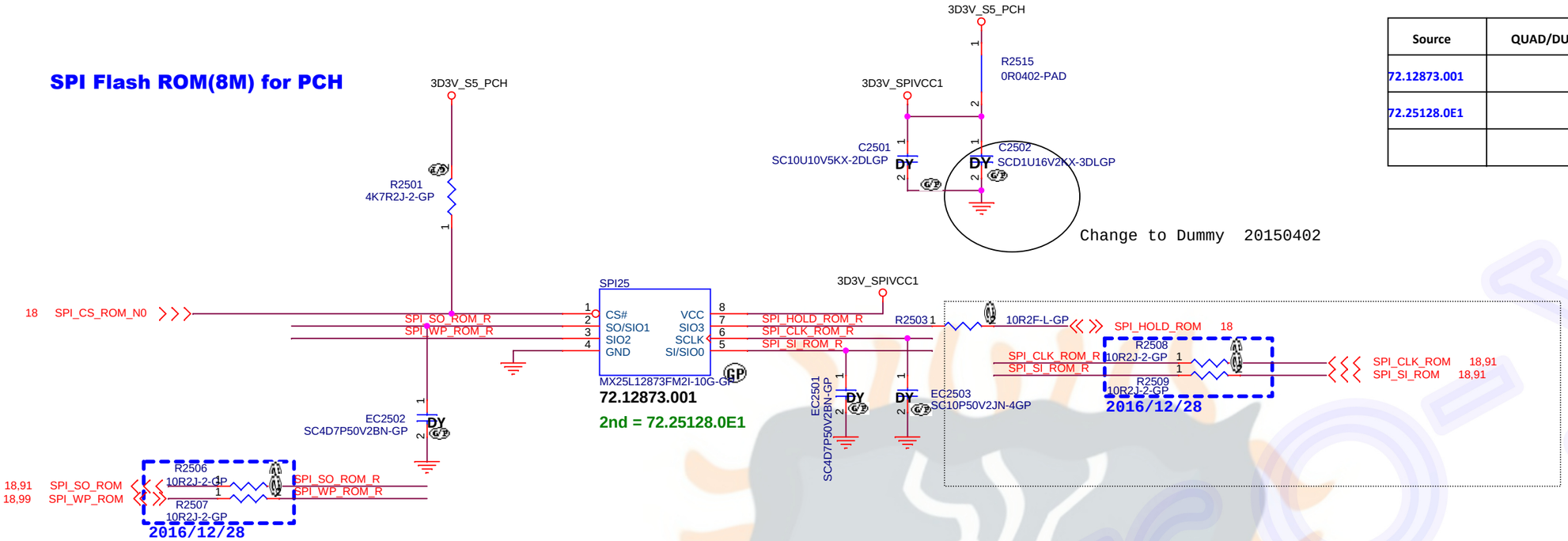
Wistron Corporation
21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE288PADX
Size: A1
Document Number: KyloRen 13"
Rev: 1.00
Date: Thursday, June 29, 2017
Sheet: 6 of 45

Eletro-X

SSID = SPI Flash

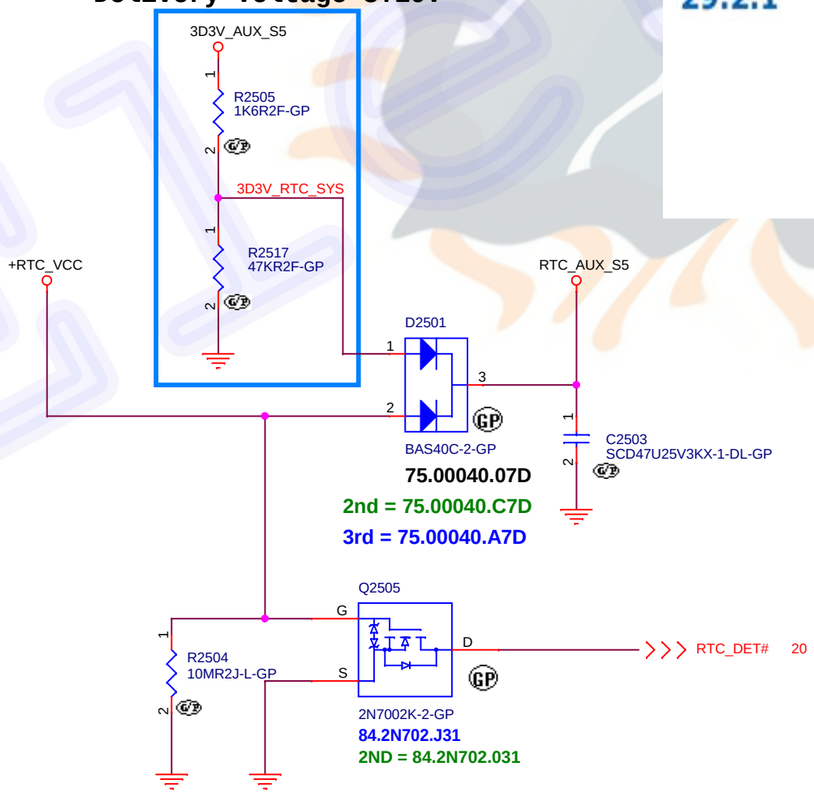
SPI Flash ROM(8M) for PCH



Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.12873.001	O	O	O
72.25128.0E1	O	O	O
	O	O	O

Main Func = RTC

Delivery Voltage 3.19V



29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

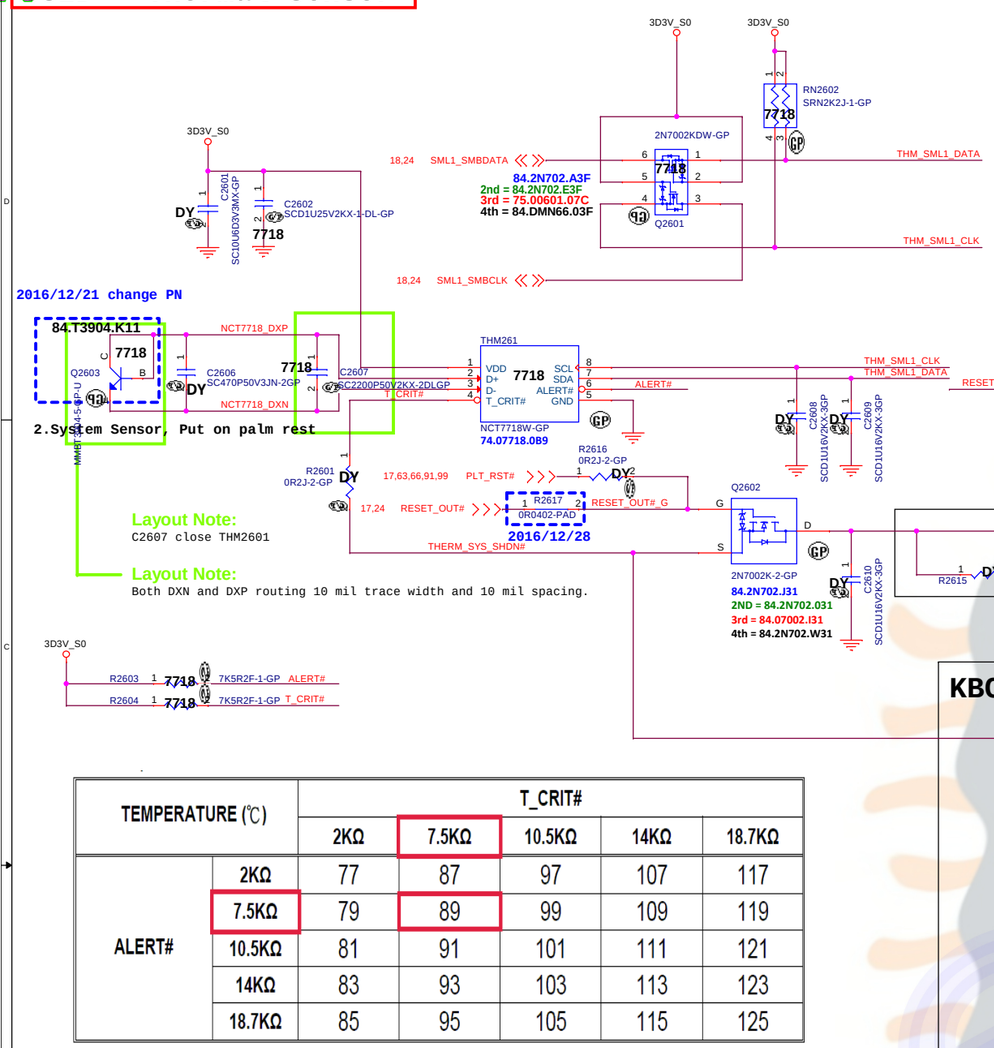
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

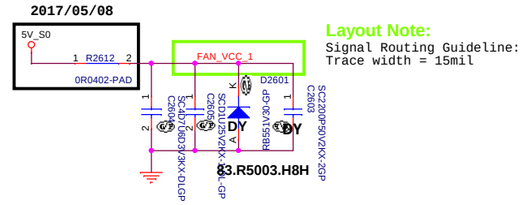
Title: Flash/RTC
Size: A3
Document Number: KyloRen 13"
Rev: A00
Date: Thursday, June 29, 2017
Sheet 25 of 106

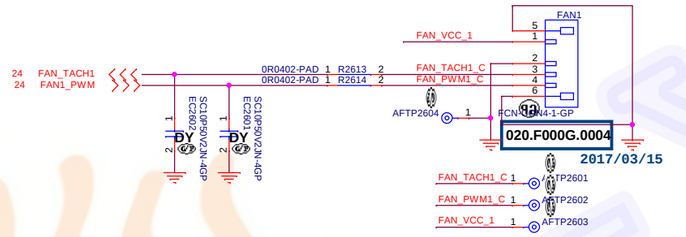
Eletro-X

SSID = Thermal Sensor

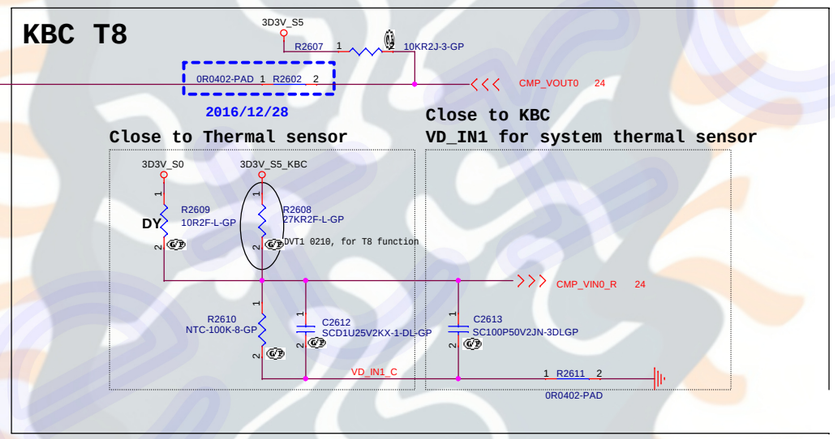


PWM FAN1





TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



Eletro-X

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.
Title
THERMAL NCT7718W/Fan
Size A2
Document Number
KyloRen 13"
Rev A00
Date: Thursday, June 29, 2017
Sheet 26

SSID = Audio

2017/05/08

3D3V_S0 — R2749 0R0603-PAD — 1D8V_S0 — R2748 DY 0R3J-0-U-GP — +3V_1D8V_AVDD

C2729 SCD1U25V2KX-1-DL-GP

C2743 SC10U6D3V3MX-DL-GP

2017/03/02

3D3V_S0 — R2751 0R0603-PAD — 1D8V_S0 — R2750 DY 0R3J-0-U-GP — +3V_1D8V_AVDD_IO

C2744 SCD1U25V2KX-1-DL-GP

C2745 SC10U6D3V3MX-DL-GP

2.5A

5V_S0 — R2707 0R0805-PAD — R2712 0R0805-PAD — +5V_PVDD

2017/03/02

C2732 SC10U6D3V3MX-DL-GP

C2742 SCD1U25V2KX-1-DL-GP

C2733 SC10U6D3V3MX-DL-GP

C2714 SCD1U25V2KX-1-DL-GP

Layout Note: Close pin41

Layout Note: Close pin46

+3V_1D8V_AVDD — R2742 100KR2J-1-GP — AUD_SENSE_A

C2746 DY SCD1U16V2KX-3DLGP

2017/05/08

1D8V_S0 — R2724 0R0603-PAD

CPVDD

C2740 SCD1U25V2KX-1-DL-GP

C2730 SC10U6D3V3MX-DL-GP

AUD_AGND

Close pin 20

+3V_1D8V_AVDD

3D3V_S0

RN1812 SRN2KJ-1-GP

2016/11/2modify

Close pin6 pin7

3D3V_AUX_S5

RTC_AUX_S5

R2728 DY 0R2J-2-GP

R2754 0R2J-2-GP

AUX_MODE

29 SPK_I2C_DATA

29 SPK_I2C_CLK

C2722 SCD1U25V2KX-1-DL-GP

+3V_1D8V_AVDD_IO

+5V_AVDD

CPVDD/AVDD2

+5V_PVDD

+5V_PVDD

5VSTB/AUX_MODE

I2C-DATA

I2C-CLK

19 HDA_CODEC_SYNC — R27271 0R0402-PAD — CODEC_BITCLK_R

19 HDA_CODEC_BITCLK — R27401 0R0402-PAD — CODEC_SDOUT_R

19 HDA_CODEC_SDOUT — R27301 0R0402-PAD — HDA_CODEC_SDIN0

19 HDA_SDIN0 — R2746 DY 0R2J-2-GP — DVSS

2017/03/02

AUDIOLINK_SYNC

AUDIOLINK_BCLK

AUDIOLINK_SDATA-OUT

AUDIOLINK_SDATA-IN

DC-DET/EAPD

Layout Note: Place close to Pin 1

+3V_1D8V_AVDD — R2744 100KR2J-1-GP — 29 AUD_SENSE — R2741 200KR2J-1-GP — AUD_SENSE_A — Audio_47

55 DMIC_DATA — R2738 0R0402-PAD — DMIC_DATA_R

55 DMIC_CLK — R2721 0R0402-PAD — DMIC_CLK_R

C2738 DY SC10P50V2JN-4DLGP

Close pin5

+3V_1D8V_AVDD — R2743 10KR2J-3-GP

24 NB_MUTE# — R2737 0R0402-PAD — EAPD#

2016/12/28

I2S-MCLK

I2S-BCLK

I2S-LRCK

I2S-IN

I2S-OUT

HP/LINE1-JD(JD1)

I2S-IN/I2S-OUT-JD(JD2)

GPIO0/DMIC-DATA12

GPIO1/DMIC-CLK

DMIC-CLK-IN/I2S-EN/SPDIF-OUT/GPIO2/DMIC-DATA34

PDB

ALC3254-CG-GP

19 SPKR

24 BEEP

RN2702 SRN1KJ-7-GP

HDA_SPKR_R

KBC_BEEP_R

D2702 BAT54C-7-F-3-GP

AUD_PC_BEEP_C

C2726 SCD1U25V2KX-1-DL-GP

AUD_PC_BEEP_R

R2745 2K2R2J-2-GP

75.00054.E7D

2nd = 83.R2003.W81

3rd = 75.00054.A7D

4th = 83.R2003.V81

moat

2017/05/04

EC2711 1 — 2 0R0402-PAD-2-GP

EC2710 1 — 2 0R0402-PAD-2-GP

DY EC2713 1 — 2 SCD1U25V2KX-1-DL-GP

EC2709 1 — 2 0R0402-PAD-2-GP

DY EC2712 1 — 2 SCD1U25V2KX-1-DL-GP

DY EC2714 1 — 2 SCD1U25V2KX-1-DL-GP

AUD_AGND

R2739 0R0805-PAD

AUD_AGND

Layout Note: R2739 should place nearby codec IC.

2016/12/28

PCBEEP — AUD_PC_BEEP — R2729 0R0402-PAD — AUD_PC_BEEP_R

MIC2-L(PORT-F-L)/RING2

MIC2-R(PORT-F-R)/SLEEVE

RING2 29

SLEEVE 29

Layout Note: Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

LINE1-L(PORT-C-L)

LINE1-R(PORT-C-R)

LINE1_L 29

LINE1_R 29

SPK-OUT-L+ — AUD_SPK_L+ 29

SPK-OUT-L- — AUD_SPK_L- 29

SPK-OUT-R+ — AUD_SPK_R+ 29

SPK-OUT-R- — AUD_SPK_R- 29

Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power

HPOUT-L(PORT-I-L) — AUD_HP1_JACK_L 29

HPOUT-R(PORT-I-R) — AUD_HP1_JACK_R 29

VREF — AUD_VREF — C2737 SC2D2U10V3KX-1DLGP-U — AUD_AGND

LDO1_CAP — C2734 SC10U6D3V3MX-DL-GP

LDO2_CAP — C2736 SC10U6D3V3MX-DL-GP

LDO3_CAP — AUD_AGND

C2731 SC10U6D3V3MX-DL-GP

100KR2J-1-GP — R2747 — AUD_AGND

MIC2-VREFO-L 29

MIC2-VREFO-R 29

MIC2-CAP — MIC_CAP — C2735 SC10U6D3V3MX-DL-GP — AUD_AGND

CPVEE — C2741 SC1U50V3KX-1-GP — AUD_AGND

CBP — C2739 SC1U50V3KX-1-GP

2016/11/3

AVSS1 — AUD_AGND

AVSS2 — AUD_AGND

GND

moat 2017/05/08

+5V_AVDD — R2705 0R0603-PAD — 5V_S0

C2721 SCD1U25V2KX-1-DL-GP

C2727 SC10U6D3V3MX-DL-GP

AUD_AGND

Layout Note: Place close to Pin 40

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3254

Size: A2 | Document Number: KyloRen 13" | Rev: 1.00

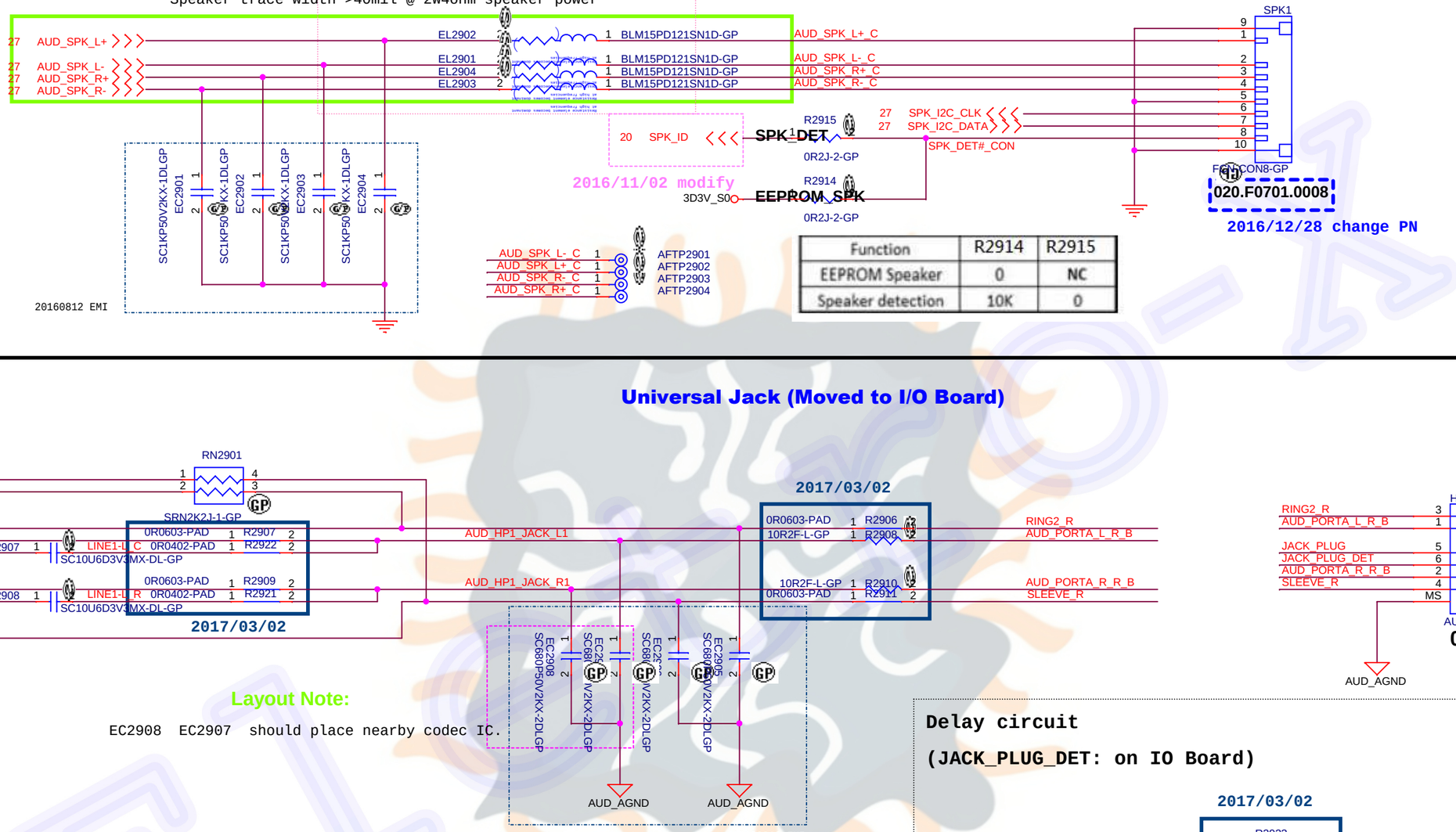
Date: Thursday, June 29, 2017 | Sheet 27 of 48

Eletro-X

SSID = Audio

Speaker

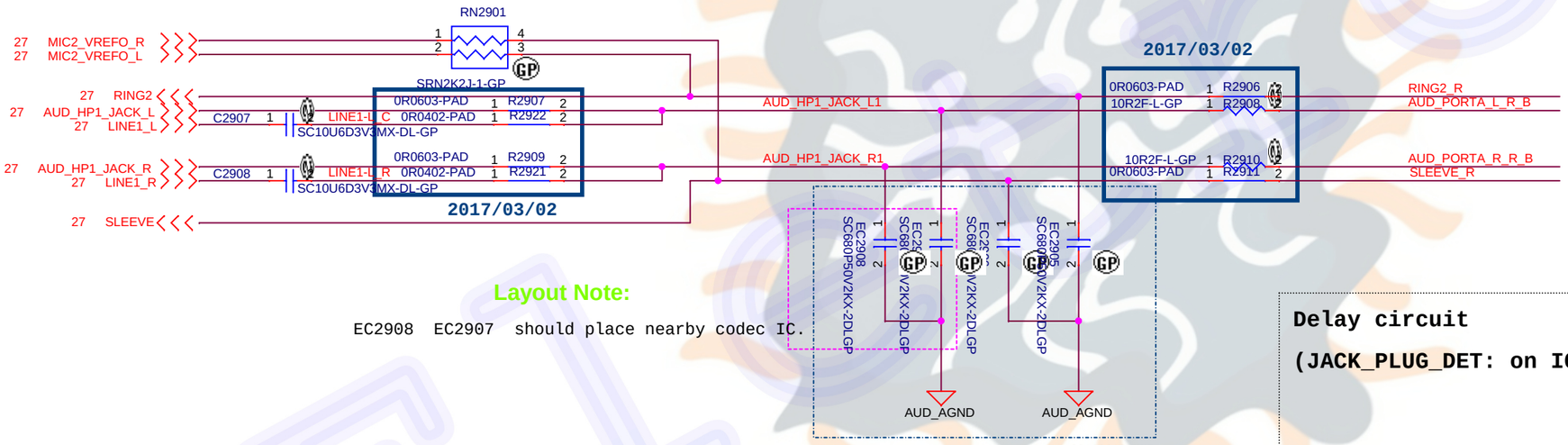
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



Function	R2914	R2915
EEPROM Speaker	0	NC
Speaker detection	10K	0

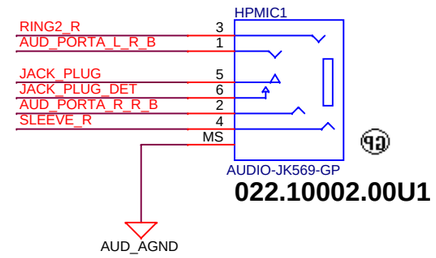
CONN Pin	Net name
Pin1	SPK_L+_C
Pin2	SPK_L-_C
Pin3	SPK_R+_C
Pin4	SPK_R-_C
Pin5	GND
Pin6	SPK_I2C_CLK
Pin7	SPK_I2C_DATA
Pin8	SPK_DET#_CON

Universal Jack (Moved to I/O Board)



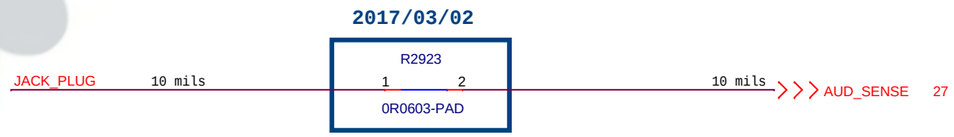
Layout Note:

EC2908 EC2907 should place nearby codec IC.

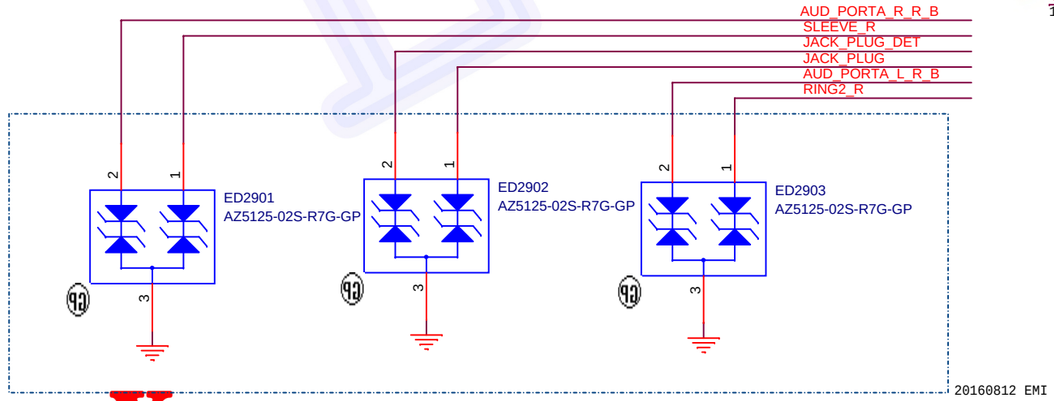


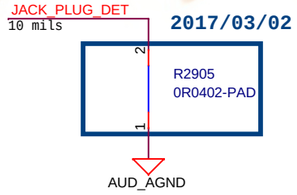
Delay circuit

(JACK_PLUG_DET: on IO Board)



CLOSS TO HPMIC1





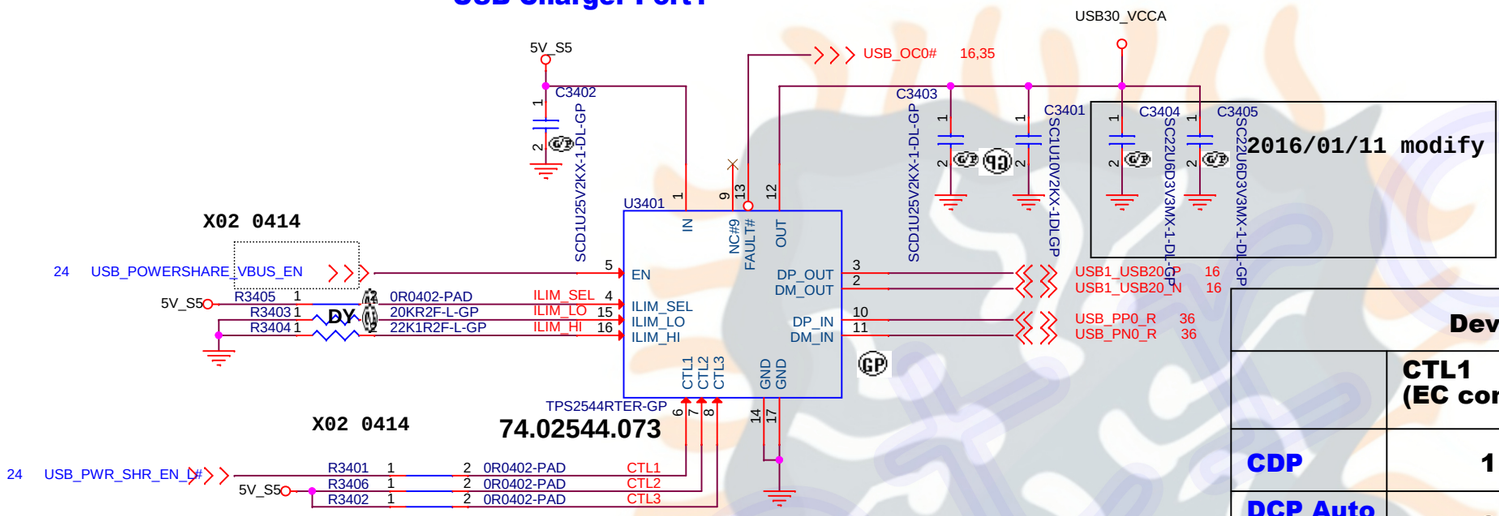
Eletro-X

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO
Size: A3
Document Number: KyloRen 13"
Rev: A00
Date: Thursday, June 29, 2017
Sheet 29 of 106

SSID = USB3.0 Port1

USB Charger Port1



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size: A3 | Document Number: KyloRen 13" | Rev: A00

Date: Thursday, June 29, 2017 | Sheet 34 of 106

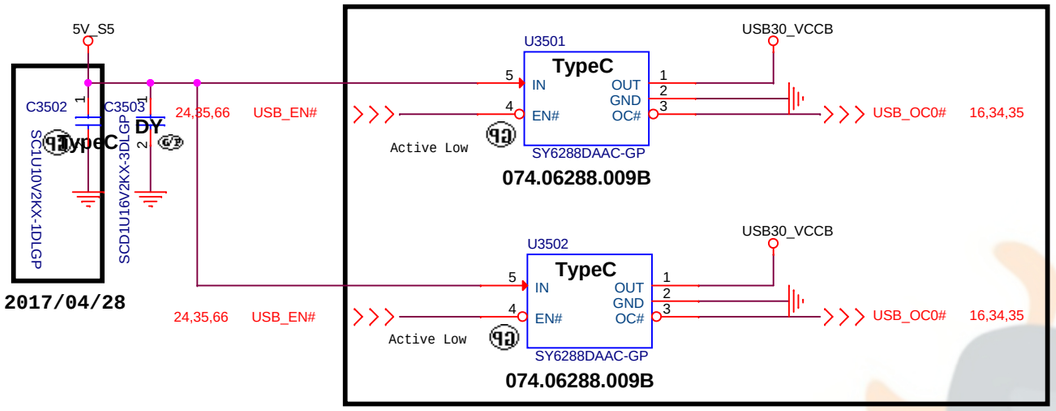
Eletro-X

SSID = USB3.0 Port1

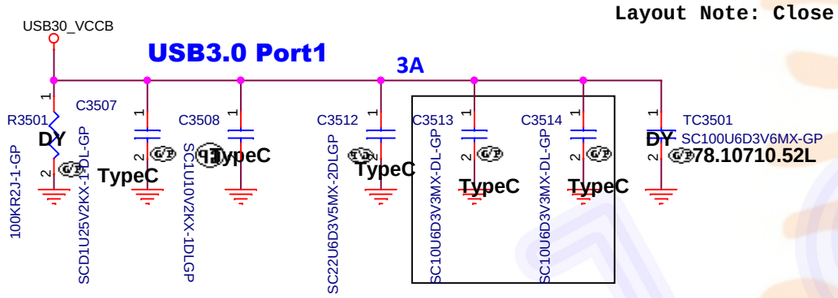
USB B Port1 Type-C

USB 3.0 Port3

2017/04/21



Layout Note: Close USB3



for starlord placement modify

USB3.0 Port3

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB switch

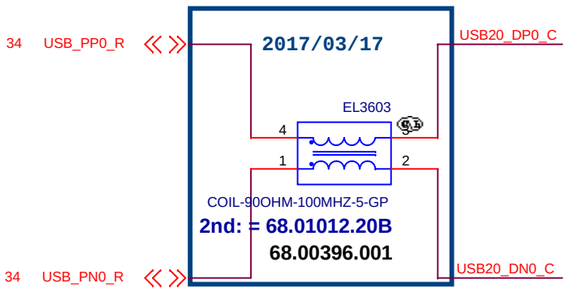
Size | Document Number: KyloRen 13" | Rev: A00

Date: Thursday, June 29, 2017 | Sheet 35 of 106

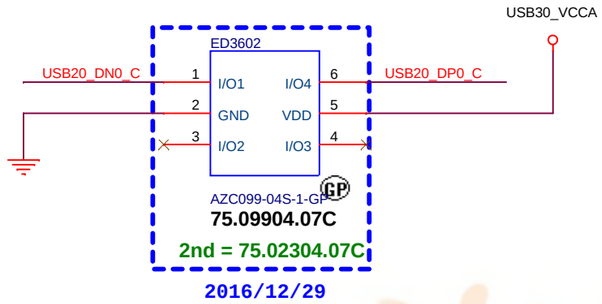
Eletro-X

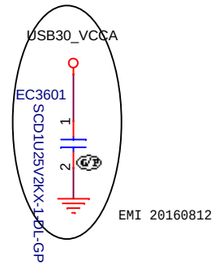
SSID = USB3.0 Port1

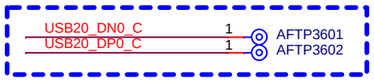
USB3.0 Port1

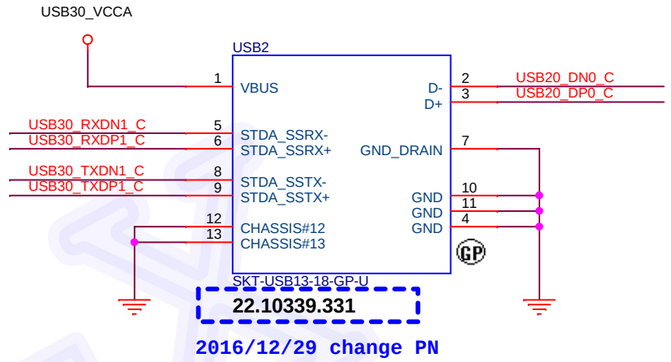


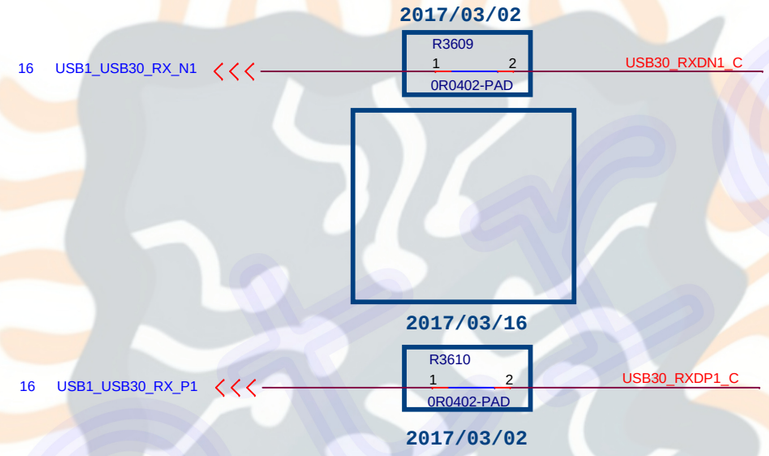
USB2.0 Port2 and USB2.0 Port3 are on IOBD

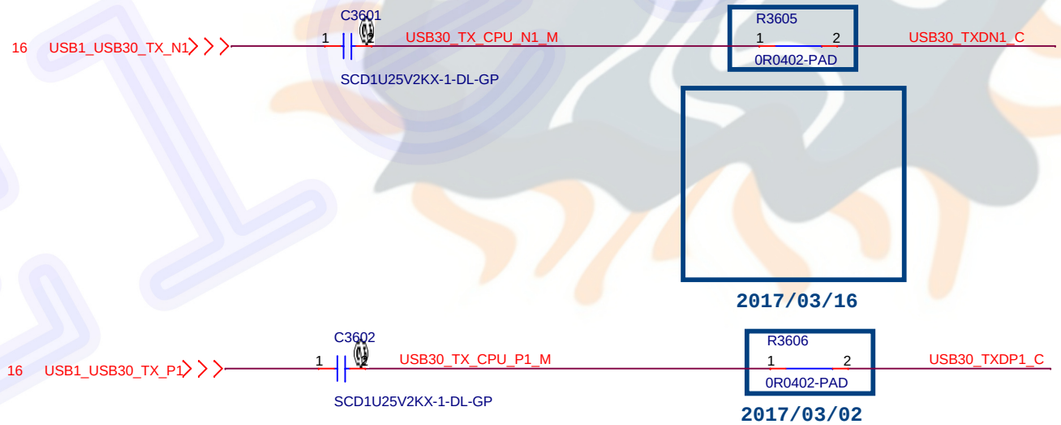


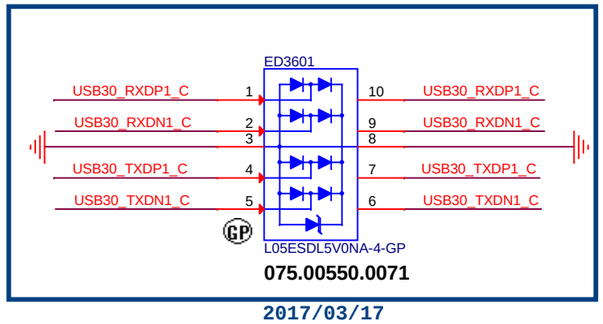












USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB30

Size: A3 | Document Number: KyloRen 13" | Rev: A00

Date: Thursday, June 29, 2017 | Sheet 36 of 106

Eletro-X

SSID = CCG4

U3701 CCG4 40-QFN

VDDD
VDDIO
VCCD
V5V_P1
NC#23
I2C_SDA_SCB2_AR/VSEL_1_P1
I2C_SCL_SCB2_AR
I2C_INT_AR_P1
GPIO#6
VBUS_MON_P1/GPIO
GPIO#37
SWD_IO/AR_RST#
SWD_CLK/I2C_CFG_EC
I2C_INT_EC
I2C_SDA_SCB1_EC
I2C_SCL_SCB1_EC
VCONN_MON_P1/GPIO
OVP_TRIP_P1
SCL_3
GPIO#27
GPIO#21
XRES
GND
VBUS_P_CTRL_P1
VBUS_C_CTRL_P1
VBUS_DISCHARGE_P1
HPD_P1/GPIO
CC2_P1
CC1_P1
SDA_3/MUX_CTRL_3_P1/VSEL_2_P1
SDA_4/MUX_CTRL_2_P1
SCL_4/MUX_CTRL_1_P1
GPIO#30
NC#22
NC#24
GPIO#34
GPIO#35
GPIO#36
GPIO#38
GPIO#39
GPIO#40

CYPD4125-40LQXIT-8-GP
071.04125.0003
2017/05/04

PD Function
PD_VBUS_P_CTRL1 43
PD_VBUS_C_CTRL1 43
PD_VBUS_DISCHG 43

2017/05/08
5V_S5
R3740 0R0603-PAD
VCC3PD
R3732 0R0603-PAD
R3733 0R0402-PAD
2017/05/08

2017/01/18
5V_VCONN_P1_IN
C3705 SCD1U25V2KX-1-DL-GP
C3704 SC10U6D3V3MX-DL-GP
C3719 SCD1U25V2KX-1-DL-GP
C3718 SC10U6D3V3MX-DL-GP

2017/04/28
U3703 AP2151DFMG-7-GP-U
074.02151.0073
R3734 100KR2F-L1-GP
5V_VCONN_EN
5V_VCONN_P1
C3715 SC1U10V2KX-1DLGP

CCG4_FLIP# 38

VCCPD_VBUS
R3730 100KR2F-L1-GP
R3726 10KR2F-2-GP
C3717 SCD1U25V2KX-1-DL-GP
PD_VBUS_R
VBUS monitor for OVP

C3701 SCD1U25V2KX-1-DL-GP
C3702 SCD1U25V2KX-1-DL-GP
C3703 SC1U10V2KX-1DLGP

RN3701 SRN2K2J-1-GP
I2C_CLK_PD
I2C_DATA_PD
RN3702 SRN2K2J-1-GP
CCG4_I2C_SCL
CCG4_I2C_SDA

2017/01/24
CCG4_I2C_INT#
CCG4_I2C_INT#_R
2017/03/02
R3731 0R0402-PAD

R3706 1MR2J-1-GP
R3735 2MR2-GP
VCONN_MON_P1
43 CCG4_OVP_TRIP_P1
2017/04/21

CCG4_ID_1
CCG4_ID_2
TP3704 TPAD14-OP-GP 1GPIO_21
R3736 30KR2F-GP
R3741 10KR2F-2-GP
R3737 10KR2F-2-GP
R3742 30KR2F-GP
R3724 4K7R2J-2-GP
C3716 SCD1U25V2KX-1-DL-GP
PD_XRES

2017/03/02
R3729 0R0402-PAD
R3727 0R0402-PAD
R3728 0R0402-PAD
R3725 10KR2F-2-GP
PL 100K to GND on CPU side
CPU_DP_HPD_MUX
CPU_DP_HPD_R 8,38
PD_CC2
USBC1_CC2_CONN 38
PD_CC1
USBC1_CC1_CONN 38

DOCK_USB_EN_A 38
I2C_DATA_PD 38
I2C_CLK_PD 38
I2C to MUX

DOCK_USB_EN_B 38
2017/01/24 modify by vendor

For Debug
TP3701 1 TPAD14-OP-GP PD_SWD_IO
TP3702 1 TPAD14-OP-GP PD_SWD_CLK
TP3703 1 TPAD14-OP-GP PD_XRES

3D3V_S5_KBC
R3707 2K2R2J-2-GP
2017/01/24
CCG4_I2C_INT#_R

For Dead Battery modify

From System 2016/11/25 change PN follow 15"
3D3V_S5
D3701 SBA0520Q-R1-00001-GP-U
VCC3PD
D3702 SBA0520Q-R1-00001-GP-U

VBUS to 3.3V
U3702 AP2204K-ADJTRG1-GP
74.02204.03F
TPS70933_EN
VREG3PD
R3701 19K6R2F-GP
R3702 10KR2F-2-GP
Vout=1.215*(1+19.6/10)=3.5964
C3707 SC1U50V3KX-1-GP
C3710 SC2D2U10V3KX-1DLGP-U
2016/12/21 modify

R3738 10KR2J-3-GP
Q3701 2N7002K-2-GP
R3739 100KR2J-1-GP
C3720 SCD22U10V2KX-2-GP
Q3701_G
TPS70933_EN
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31

For Dead Battery modify

USBC1_CC1_CONN
USBC1_CC2_CONN
C3711 SC390P50V2KX-1-GP
C3712 SC390P50V2KX-1-GP

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: (Reserved)
Size: A3
Document Number: KyloRen 13"
Rev: A00
Date: Thursday, June 29, 2017
Sheet 37 of 106

Eletro-X

SSID = TYPEC MUX

DisplayPort Source

USB HOST

U3801 TUSB546-DCIRNQP-GP

071.00546.0003

2016/11/25 change PN

2016/10/31modify

FLIP POL	CTL0 AMSEL	CTL1 EN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

	DCI	non-DCI
23 CTL1/HPDIN	DP ENABLE in GPIO mode HPD in I2C mode	DP Enable in GPIO mode, Unused in I2C mode
29 CAD_SNK/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode	HPD

U3802 TS3DS10224RUKR-GP

071.10224.0003

TypeC

2017/05/08

2017/05/17

2017/03/02

2017/03/16

EL3801 EL3802 COIL-90OHM-100MHZ-SGP

68.00396.001

2nd: = 68.01012.20B

FLIP#	ENA	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	I2C	USB
1	1	0	USB	X
1	1	1	USB	I2C

ED3801 ED3802 L05ESDL5V0NA-4-GP

075.00550.0071

TypeC

2017/03/17

ED3803 ED3804 ED3805 ED3806 AZ5315-02F-GP

83.05315.0A0

USB1 SKT-USB34-20-GP-U

022.10005.M022

2017/05/04

2016/12/07 add AFTP

2016/12/16 add AFTP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size: A2 | Document Number: KyloRen 13" | Rev: A00

Date: Thursday, June 29, 2017 | Sheet 38 of 56

Eletro-X

SSID = Power Plane & Sequence

ROSA Run Power

2016/12/16 add AFTP

3D3V_S0 1 AFTP4001
3D3V_S0 1 AFTP4002
5V_S5 1 AFTP4003
5V_S5 1 AFTP4004

2017/05/08

2016/12/07 for power sequence

D4005 83.R2004.G8F
RB751V-40H-GP
2017/03/02
17,24,40,51 SIO_SLP_S3# 3V5V_S0_ON
R4010 0R0402-PAD
C4003 SCD22U10V2KX-2-GP
2016/11/28 for power sequence
2016/12/06 for power sequence

U4001
G5016KD1U-GP
074.05016.0093
5V_S5 3D3V_S5
VBIAS IN1#1 IN1#2 EN1 IN2#6 IN2#7 EN2
OUT1#13 OUT1#14 CT1 OUT2#8 OUT2#9 CT2 GND GND
3V5V_CT1 3V5V_CT2
C4002 SCD01U50V2KX-1DLGP
C4001 SCD01U50V2KX-1DLGP

PWR_3D3V_S0 R4012 3D3V_S0
0R0603-PAD
C4005 SC10U25V5KX-DL-GP
PWR_5V_S0 R4013 5V_S0
0R0603-PAD
C4004 SC10U25V5KX-DL-GP

5V_S0
5V_S0 Comsumption
Peak current 5A

3D3V_S0
3D3V_S0 Comsumption
Peak current 2.5A

45 3V_5V_EN
D4001 LBAS16LT1G-GP
PURE_HW_SHUTDOWN# 26
R4006 20KR2F-L-GP
83.00016.P11
R4009 10KR2J-3-GP ALWON 24
C4009 SC10U6D3V2MX-DL-GP
DVT1 0210
modify at DVT1 power sequence 20150203

Power Good

D4003 2016/12/29
SIO_SLP_S3# 83.R2004.G8F
RB751V-40H-GP
R4011 0R0402-PAD
51 1D2V_VTT_PWRGD
D4002 RSMRST_PWRGD# DY
RB751V-40H-GP 83.R2004.G8F
[#543016] Optional, Added for addition system robustness

3D3V_S0 R4005 100KR2J-1-GP 2017/03/16
RUNPWROK 17,24
R4002 0R0402-PAD VR_EN 46
3D3V_S5 3D3V_S5_KBC
R4031 100KR2J-1-GP R4032 100KR2J-1-GP DY
RSMRST_PWRGD#

2017/01/24
52 1D0V_S5_PWRGD
24,54 PRIM_PWRGD
17,45,52,54 3V_5V_POK
R4029 R4030 R4033 0R2J-2-GP 0R0402-PAD
2016/12/13
NON DS3: PH 3V_5V_POK to 3D3V_AUX_S5 at page17

VCCIO and VCCSTG

2016/12/29
D4004 83.R2004.G8F
RB751V-40H-GP
2016/12/29
R4017 47KR2J-L2-GP DY
3D3V_S0 R4003 10KR2J-1-GP
5V_S5 C4032 SCU1U10V2KX-1DLGP
1D0V_S5 C4006 SC10U6D3V3MX-DL-GP C4035 SC22U6D3V3MX-1-DL-GP C4036 SC22U6D3V3MX-1-DL-GP

3D3V_S5
U4007 TC7SZ08FU-LJ-CT-GP
073.7SZ08.000G DY
2016/12/16 DY
17,24,40,51 SIO_SLP_S3#
17,24,91 SIO_SLP_S0#
VCCSTG_EN_L R4037 0R2J-2-GP DY
VCCSTG_EN_R

U4002 APE8939GN3-GP
074.08939.0093
VIN VIN VBIAS EN VOUT#8 VOUT#7 VOUT#6 GND VIN
C4033 SCD1U25V2KX-1-DL-GP DY

2017/05/08
+VCCIO_SIP +VCCIO R4045 0R1206-PAD
+VCCSTG R4042 0R0603-PAD
C4007 SCD1U25V2KX-1-DL-GP

2016/12/07 for power sequence

EOPIO and EDRAM

+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

+V1.8V_S0

+V1.8A
Q4002 DMP2130L-7-GP
1D8V_S0
150mA
C4037 SCD1U25V2KX-1-DL-GP
R4034 10KR2J-3-GP
C4038 SC1U10V2KX-1DLGP
R4035 20KR2J-L2-GP
1D8V_EN_R#
C4039 SCD1U16V2KX-3GP DY
17,24,40,51 SIO_SLP_S3#
Q4001 2N7002K-2-GP
1D8V_EN#
84.02130.031
2nd = 84.00102.031
3rd = 84.03413.B31

MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

2016/12/12 for power sequence

1D0V_S5
C4013 SC10U25V5KX-DL-GP
17,54 SIO_SLP_S4#
R4024 0R0402-PAD
VCCSTU_EN_R
5V_S5
C4034 SCD1U25V2KX-1-DL-GP DY
C4031 SC1U10V2KX-1GP DY

U4006 APE8937GN2-GP-U
074.08937.0093
VIN VIN EN VBIAS VOUT#8 VOUT#7 CT GND GND
U4006_CT
C4017 SC2K2X7R1D1SCS DY
+V1.00U_CPU
C4012 SC10U6D3V3MX-DL-GP

2017/05/08
R4036 0R0603-PAD +VCCST_CPU
R4038 0R0603-PAD +VCCSFR 0.04 A

<Core Design>

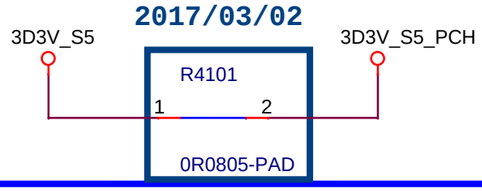
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable
Size: A2
Document Number: KyloRen 13"
Rev: A00
Date: Thursday, June 29, 2017
Sheet 40 of 56

Eletro-X

SSID = Power Plane & Sequence

2017/03/02



Reserve by NON DS3 function 20150413

DS3

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Connected_Standby(1/2)+DS3*	
Size: A4	Document Number: *KyloRen 13"*	Rev: *A00*
Date: Thursday, June 29, 2017	Sheet 41 of 106	

Eletro-X

Main Func = ADT Input

Pin Definition: TBD

Layout Note:
PSID Layout width > 25mil

2016/12/21 change PN
84.T3904.K11
PQ4302 MMBT3904-5-GP-U
84.05067.031
PQ4301 DMN5L06K-7-GP
PD4303 L30ESD24VC3-2-GP
PD4302 LBAV99LT1G-1-GP
75.00099.O7D
2nd = 75.00099.K7D
3rd = 75.00099.Q7D
4th = 75.00099.D7D

2017/06/20
PD4304 BAT54C-7-F-3-GP
75.00054.E7D

2017/03/16
20140815 david
020.F000F.0008
2017/03/15
2016/01/07 mofiy
83.P6SMB.JAG

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA
2017/03/16

2016/11/29 SC要follow 15"
2016/12/06 follow 15"

20161226
PU4301 AON7403-GP-U 84.07403.037
20161031
PU4302 AON7403-GP-U 84.07403.037
NON_TypeC
2016/12/27 change PN
PD4305 RB751V-40H-GP
If=0.3A
PQ4305 LTA024EUB-FS8-GP 84.00024.01K
PQ4304 LMUN5212T1G-GP 84.05212.B11

2017/06/20
73.01G04.01V
2017/03/15

2017/04/21
PQ4313 2N7002KDW-GP 84.2N702.A3F
PD4308 RB751V-40H-GP

2017/06/12
PU4303 AON7403-GP-U 84.07403.037
PU4304 AON7403-GP-U 84.07403.037

2017/03/08
2017/06/20
074.01004.00BF
2017/04/25
VBUS_C_CTRL = 1 (Consumer Path ON)
VBUS_C_CTRL = 0/Z (Consumer Path OFF)
2N7002K-2-GP 84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31
4th = 84.2N702.W31
VBUS overvoltage output indicator (active LOW)
2017/06/17
PD_VBUS_DISCHG = 1 (VBUS Discharging)
PD_VBUS_DISCHG = 0/Z (VBUS not discharging)
If=0.3A

PU4305 PU4306 SI7625DN-T1-GE3-GP 84.07625.037
PD_VBUS_P_CTRL1 = 1 (Provider Path ON)
PD_VBUS_P_CTRL1 = 0/Z (Provider Path OFF)
20161226 2017/03/02
Id=115mA
VBUS overvoltage output indicator (active LOW)

Main Func = M-BAT Input

Placement: Close to Batt Connector 2017/03/21
ED4301 LBAV99LT1G-1-GP 75.00099.O7D
ED4302 LBAV99LT1G-1-GP 75.00099.O7D
ED4303 LBAV99LT1G-1-GP 75.00099.O7D
2nd = 75.00099.K7D | 2nd = 75.00099.K7D | 2nd = 75.00099.K7D
3rd = 75.00099.Q7D | 3rd = 75.00099.Q7D | 3rd = 75.00099.Q7D
4th = 75.00099.D7D | 4th = 75.00099.D7D | 4th = 75.00099.D7D

Batt Connecter
020.F0867.0010
2017/03/07
2017/01/24

2017/05/10
2017/05/12
U4301 074.01004.00BF
VCCPD_VBUS>5.4V VBUS_PRODECT=H
VCCPD_VBUS<5.4V VBUS_PRODECT=L
Vth(max)=1V
need check

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.
Title: DCIN
Size: A2 | Document Number: KyloRen 13" | Rev: A00
Date: Thursday, June 29, 2017 | Sheet 43 of

Eletro-X

Main Func = Charger

75.87333.071 CSD87330
HS-
Vgs @ 5V,
Id = 15A,
Rds(on) = 9.45mohm,
LS-
Vgs @ 5V,
Id = 15A,
Rds(on) = 3.6mohm,

2.2uH,
DCR=14~16.5mohm,
Idc=8.5A, Isat=11A
10.3*11.2*4.4mm

84.07121.037 SI7121DN
Rds(on) = 24~30 mohm,
Vgs=10V, I-D = 12A,
Qg = 43nC
Vgs=± 25V, Vds=-30V,
I-D=-16A

074.09538.0073

2016/12/29 change PN
75.00054.E7D
2nd = 83.R2003.V81
3rd = 75.00054.A7D
4th = 83.R2003.V81

2016/12/29 change PN
83.R2004.G8F
75.00054.E7D
2nd = 83.R2003.V81
3rd = 75.00054.A7D
4th = 83.R2003.V81

2016/12/29 change PN
75.00054.E7D
2nd = 83.R2003.V81
3rd = 75.00054.A7D
4th = 83.R2003.V81

84.2N702.A3F
2nd = 84.DM601.03F
3rd = 84.2N702.E3F
4th = 84.2N702.F3F

84.2N702.A3F
2nd = 75.00601.07C

84.T3906.A11
2nd = 84.03906.P11

84.2N702.A3F
2nd = 84.DM601.03F
3rd = 84.2N702.E3F
4th = 84.2N702.F3F

Check with DELL

CHECK EE
follow custormer circuits.

PU +VCCSTG = 1.0 V on CPU side

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ)			CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
MIN	TYP 1%	MAX				
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	Yes	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	Yes	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476

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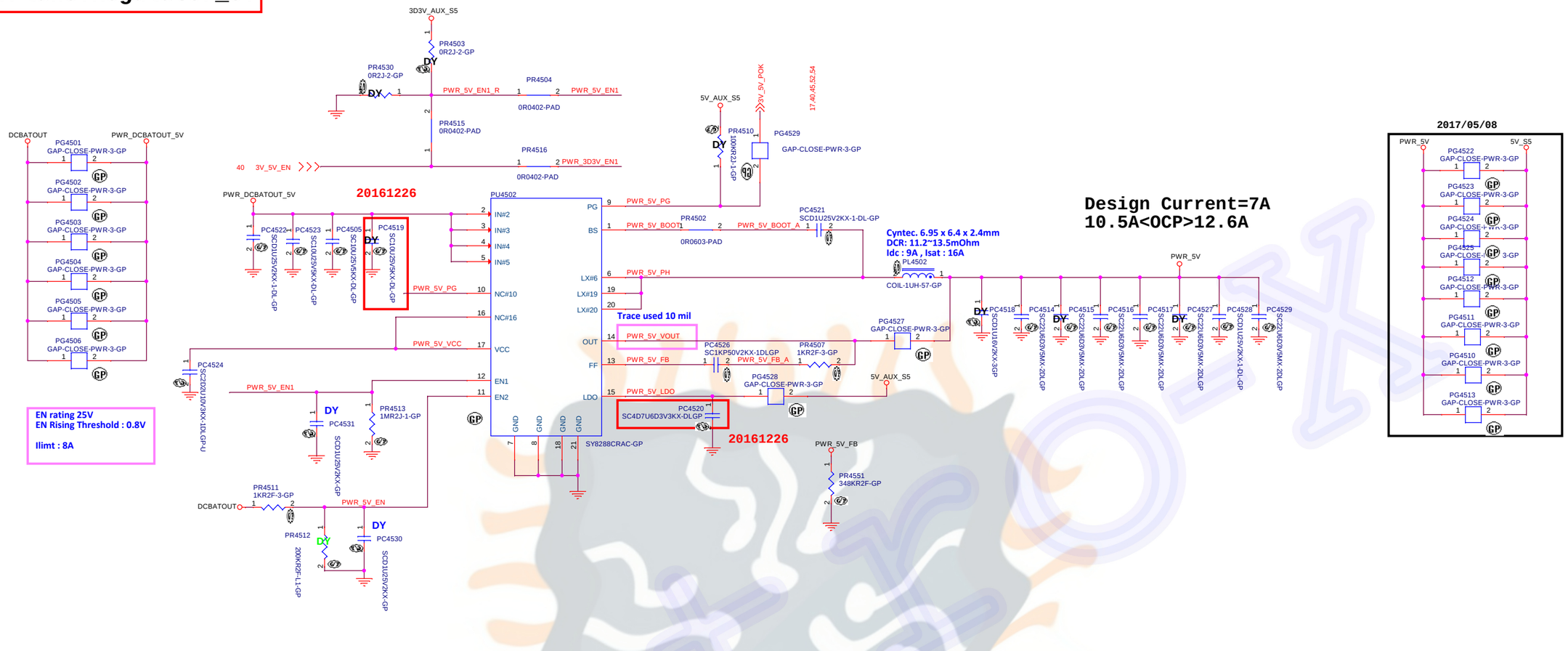
VIEW ONLY

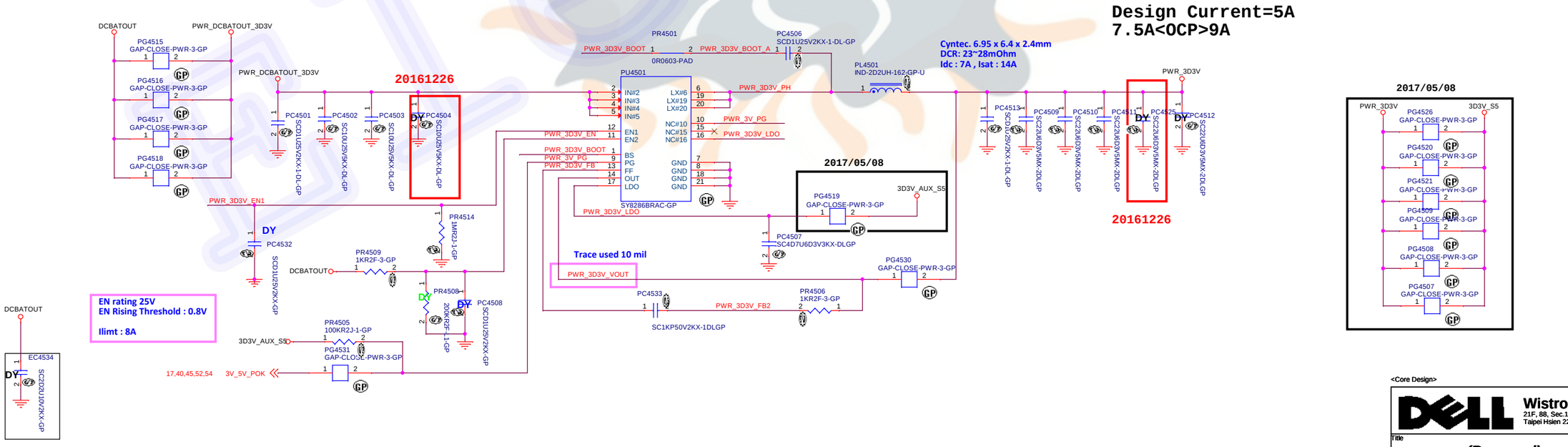
Eletro-X

<Core Design>
DELL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: Charger
Size: A1
Document Number: KyloRen 13"
Rev: A00
Date: Thursday, June 29, 2017
Sheet: 45 of 51

SSID = PWR.Plane.Regulator_5V



SSID = PWR.Plane.Regulator_3D3V



RF request 2016/01/12 modify

Eletro-X

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)
Size: A2 | Document Number: KyloRen 13" | Rev: A00
Date: Thursday, June 29, 2017 | Sheet 45 of 105

Main Func = CPU_CORE

	U22	U42
PC4614	330P(78.33124.2FLDL)	470p(78.47124.2FLDL)
PC4618	1KP(78.10224.2FLDL)	470p(78.47124.2FLDL)
PC4625	DY	0.022u(78.22321.2FLDL)
PC4626	DY	0.022u(78.22321.2FLDL)
PR4669	DY	DY
PR4635	1K(64.10015.6DL)	DY
PR4642	357(64.35705.6DL)	464 (64.46405.6DL)
PC4630	47nF(078.47322.02FD)	47nF(078.47322.02FD)
PC4628	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)
PC4654	10nF(78.10324.2FLDL)	10nF(78.10324.2FLDL)
PC4653	DY	47nF(078.47322.02FD)
PR4633	1.54K(64.15415.6DL)	3.01K(64.30115.6DL)
PR4608	90.9K(64.90925.6DL)	95.3K (64.95325.6DL)

2017/02/21
2017/06/06
2017/04/25

Eletro-X

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., HsiChih
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81208MN_CPU_VCORE(1/3)
Size: A2 | Document Number: KyloRen 13" | Rev: A00
Date: Thursday, June 29, 2017 | Sheet 46 of 106

SSID = CPU_CORE

DCBATOUT

PWR_DCBATOUT_VCORE

PG4701 GAP-CLOSE-PWR-GP
PG4702 GAP-CLOSE-PWR-GP
PG4703 GAP-CLOSE-PWR-GP
PG4704 GAP-CLOSE-PWR-GP
PG4705 GAP-CLOSE-PWR-GP
PG4706 GAP-CLOSE-PWR-GP

PWR_DCBATOUT_VCORE

PC4701 SC10U25V5KX-DL-GP
PC4702 SC10U25V5KX-DL-GP
PC4703 SC10U25V5KX-DL-GP
PC4704 SC10U25V5KX-DL-GP

PR4706 0R0402-PAD-1-GP
46 PWR_VCORE_FCCM#

5V_S5
PR4704 2D2R2F-GP
PC4708 SC1U10V2KX-1DLGP

PR4702 0R0402-PAD-1-GP
PWR_VCORE_PWM 46

PR4712 5K11R2F-L1-GP
PWR_VCORE_BOOT_RC
PR4705 2D2R3F-L-GP
PC4707 SCD22U25V3KX-DL-GP

PU4701
PWR_VCORE_FCCM#_R
PWR_VCORE_VCC_R
PWR_VCORE_SW
SKIP# VDD PGND VSW
PWM BOOT BOOT_R VIN PGND
PWR_VCORE_PWM_R
PWR_VCORE_BOOT
PWR_VCORE_BOOTR
PWR_DCBATOUT_VCORE
CSD97396Q4M-GP
074.97396.0043

PL4701
COIL-D15UH-8-GP
+VCCGT

PR4703 2D2R6J-3-GP
DY
PWR_VCORE_SNB
PC4706 SC1KP50V2KX-L-1-GP
DY

PG4707 GAP-CLOSE-PWR-3-GP
PG4708 GAP-CLOSE-PWR-3-GP
PWR_VCORE_ISUMP_G
PWR_VCORE_ISUMN_G

PR4708 3K65R2F-1-GP
PR4701 0R0402-PAD-1-GP

PT4701 SE330U2VDM-4-GP
PANASONIC
ESR: 9 mohm

46 PWR_VCORE_ISUMP
46 PWR_VCORE_ISUMN

SKL_U22_15W
Icc(max)=29A
TDC=21A

Confirm with EE
22uF/0805 total 33pcs
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx2.4mm
DCR: 0.92m Ohm +/- 7%
Idc : 32A , Isat : 41A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCORE(2/3)
Size: A3
Document Number: KyloRen 13"
Rev: A00
Date: Thursday, June 29, 2017
Sheet 47 of 106

Eletro-X

Main Func = CPU_CORE

DCBATOUT
PWR_DCBATOUT_VCCGTA
PG4802 GAP-CLOSE-PWR-3-GP
PG4803 GAP-CLOSE-PWR-3-GP
PG4804 GAP-CLOSE-PWR-3-GP
PG4805 GAP-CLOSE-PWR-3-GP
PG4806 GAP-CLOSE-PWR-3-GP

PWR_DCBATOUT_VCCGTA
PC4802 PC4803 PC4804 PC4805
SC101U25V5KX-DL-GP

PR4806 0R0402-PAD-1-GP
46,48 PWR_VCCGT_FCCM#
5V_S5
PR4803 2D2R2F-GP
PC4809 SC1U10V2KX-1DLGP

PU4801
PWR_VCCGT_FCCM# RA
PWR_VCCGT_VCCDA
PWR_VCCGT_SWA
SKIP# VDD PGND VSW
PWM BOOT BOOT_R VIN PGND
PWR_VCCGT_BOOTA
PWR_VCCGT_BOOTRA
PWR_DCBATOUT_VCCGTA
CSD97396Q4M-GP
074.97396.0043

PR4802 0R0402-PAD-1-GP
PWR_VCCGT_PWMA 46
PWR_VCCGT_PWMA_RA
PR4817 5K11R2F-L1-GP
PR4804 2D2R3-1-U-GP
PC4808 SCD22U25V3KX-DL-GP
PWR_VCCGT_BOOTA_RC

KBL_U42_15W
Icc(max)=64A
TDC=42A

Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx2.4mm
DCR: 0.92m Ohm +/- 7%
Idc : 32A , Isat : 41A

PL4801
COIL-D15UH-8-GP
VCC_CORE

PR4805 2D2R6J-3-GP
PWR_VCCGT_SNB1
PC4810 SC1KP50V2KX-L-1-GP
PG4808 GAP-CLOSE-PWR-3-GP
PG4809 GAP-CLOSE-PWR-3-GP
PT4801 SE330U2VDM-4-GP
PANASONIC
ESR: 9 mohm

PWR_VCCGT_ISUMN_GA
PWR_VCCGT_ISUMP_GA
46,48 PWR_VCCGT_ISEN1
46,48 PWR_VCCGT_ISUMP
46,48 PWR_VCCGT_ISUMN
46,48 PWR_VCCGT_ISEN2
U42
PR4821 100KR2F-L1-GP
PR4808 3K65R2F-1-GP
PR4809 10R2F-L1-GP
PR4822 100KR2F-L1-GP

2016/12/29 DY
DCBATOUT
DY PT4805 SE33U25VM-11-GP
DY PT4806 SE33U25VM-11-GP
For acoustic noise

DCBATOUT
PWR_DCBATOUT_VCCGTB
PG4810 GAP-CLOSE-PWR-3-GP
PG4811 GAP-CLOSE-PWR-3-GP
PG4812 GAP-CLOSE-PWR-3-GP
PG4813 GAP-CLOSE-PWR-3-GP
PG4814 GAP-CLOSE-PWR-3-GP

PWR_DCBATOUT_VCCGTB
PC4814 PC4815 PC4816 PC4817
SC101U25V5KX-DL-GP

PR4812 0R0402-PAD-1-GP
46.48 PWR_VCCGT_FCCM#
5V_S5
PR4813 2D2R2F-GP
PC4812 SC1U10V2KX-1DLGP

PU4802
PWR_VCCGT_FCCM# RB
PWR_VCCGT_VCCDB
PWR_VCCGT_SWB
SKIP# VDD PGND VSW
PWM BOOT BOOT_R VIN PGND
PWR_VCCGT_BOOTB
PWR_VCCGT_BOOTRB
PWR_DCBATOUT_VCCGTB
CSD97396Q4M-GP
074.97396.0043

PR4811 0R0402-PAD-1-GP
PWR_VCCGT_PWMB 46
PWR_VCCGT_PWMB_RA
PR4818 5K11R2F-L1-GP
PR4810 2D2R3-1-U-GP
PC4811 SCD22U25V3KX-DL-GP
PWR_VCCGT_BOOTB_RC

Cyntec. 6.8mm x7.6mmx2.4mm
DCR: 0.92m Ohm +/- 7%
Idc : 32A , Isat : 41A

PL4802
COIL-D15UH-8-GP
VCC_CORE

PR4814 2D2R6J-3-GP
PWR_VCCGT_SNB2
PC4813 SC1KP50V2KX-L-1-GP
PG4813 GAP-CLOSE-PWR-3-GP
PG4815 GAP-CLOSE-PWR-3-GP
PT4803 SE330U2VDM-4-GP
20161031

PWR_VCCGT_ISUMN_GB
PWR_VCCGT_ISUMP_GB
46,48 PWR_VCCGT_ISEN2
46,48 PWR_VCCGT_ISUMP
46,48 PWR_VCCGT_ISUMN
46,48 PWR_VCCGT_ISEN1
PR4823 100KR2F-L1-GP
PR4816 3K65R2F-1-GP
PR4815 10R2F-L1-GP
PR4824 100KR2F-L1-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCCGT(3/3)
Size: A2 | Document Number: KyloRen 13" | Rev: A00
Date: Thursday, June 29, 2017 | Sheet 48 of 106

Eletro-X

SSID = CPU_CORE

PWR_DCBATOUT_VCCSA 1 AFTP5001

2017/03/16

2016/12/14 remove PT5001

DCBATOUT

PWR_DCBATOUT_VCCSA

PG5002
GAP-CLOSE-PWR-3-GP

PG5003
GAP-CLOSE-PWR-3-GP

SKL_U22_15W
Icc(max)=4.5A
TDC=3.7A

Confirm with EE
22uF/0805 total 6pcs
(78.22610.L2L)

PWR_DCBATOUT_VCCSA

PC5002 SC10U25V5KX-DL-GP

PC5003 SC10U25V5KX-DL-GP

PC5004 SCD1U25V2KX-1-DL-GP

PU5002
AON7410-GP

PWR_VCCSA_BST_RC

PR5001
2D2R3F-L-GP

PC5005
SCD22U25V3KX-DL-GP

PU5001

PWR_VCCSA_DRVH
PWR_VCCSA_BST
PWR_VCCSA_SW

UGATE
BOOT
PWM
GND
PHASE
FCCM
VCC
LGATE
GND

46 PWR_VCCSA_PWM

5V_S5

PWR_VCCSA_FCCM 46

PC5001
SC2D2U10V3KX-1DLGP-U

ISL95808HRZ-T-1-GP

074.95808.0B73

If no need support PS4 mode
please change to ISL6208C
74.06208.B73

PWR_VCCSA_DRVL

PU5003
AON7410-GP

Cyntec. 7.3mm x6.8mm x2.4mm
DCR: 4.5~5.1 mohm
Idc : 15A , Isat : 22A

2017/05/10

PL5001
COIL-D47UH-20-GP

+VCCSA

PG5011
GAP-CLOSE-PWR-3-GP

PG5001
GAP-CLOSE-PWR-3-GP

PWR_VCCSA_ISUMP_R

PWR_VCCSA_ISUMN_R

PR5003
3K65R2F-1-GP

PR5004
0R0402-PAD-1-GP

46 PWR_VCCSA_ISUMP

46 PWR_VCCSA_ISUMN

<Core Design>

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Title: VCCSA

Size: A3 | Document Number: KyloRen 13" | Rev: A00

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Eletro-X

SSID = PWR.Plane.Regulator_1D2V/0D6V

SY8288RAC for 1D2V

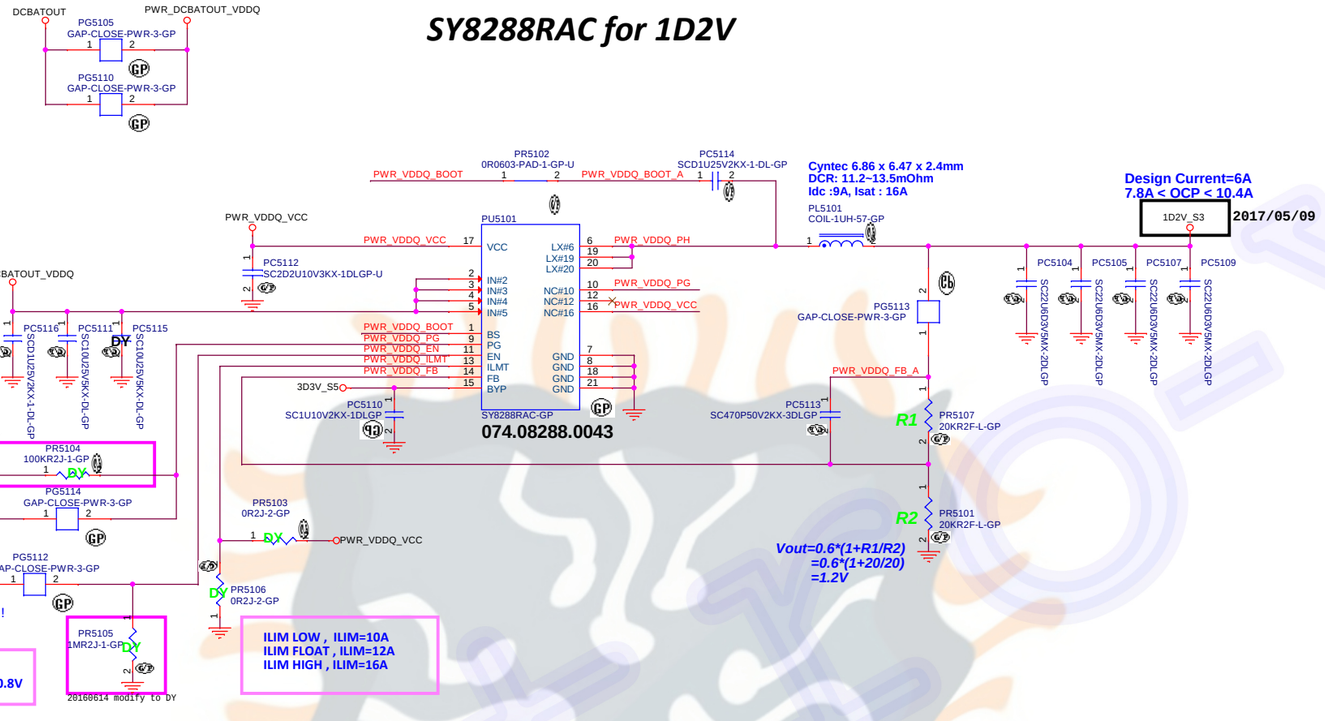
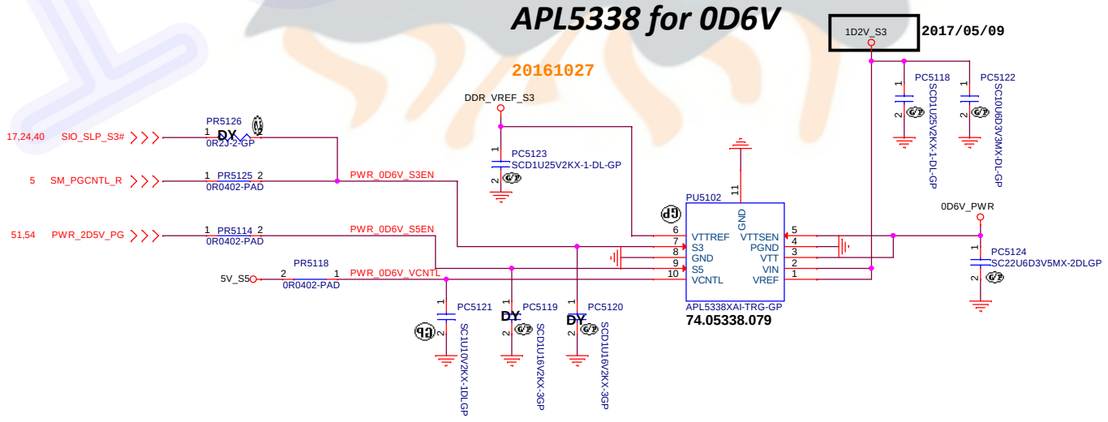


Table1. The Truth Table of S3 and S5 pins

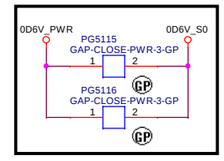
STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)

APL5338 for 0D6V

20161027



Design Current = 1470mA
2017/05/08



EE needs check it!!

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Eletro-X

SSID = PWR.Plane.Regulator_1D0V

AOZ2262 for 1D0V

2016/12/16

DCBATOUT
PWR_DCBATOUT_1D0V
PG5214 GAP-CLOSE-PWR-3-GP
PG5210 GAP-CLOSE-PWR-3-GP
PG5212 GAP-CLOSE-PWR-3-GP

1D0V_PWR
1D0V_S5
PG5201 PG5202 PG5203 PG5204 PG5205 PG5206 PG5207 PG5208 PG5209 PG5211
GAP-CLOSE-PWR-3-GP

5V_S5
PC5202 SC1U10V2KX-1DLGP

PWR_DCBATOUT_1D0V
PC5214 SCD1U50V3KX-DL-GP
PC5216 SC10U25V5KX-DL-GP
PC5211 SC10U25V5KX-DL-GP
PC5210 SC10U25V5KX-DL-GP
PC5209 SC10U25V5KX-DL-GP

PR5201 88K7R2F-GP

PU5201
AOZ2262QI-10-GP-U
074.02262.0043

21	VCC	LX#18	18 PWR_1D0V_PH
7	IN#7	LX#17	17
8	IN#8	LX#16	16
9	IN#9	LX#11	11
		LX#10	10
20	BST		PWR_1D0V_BT
5	FB		PWR_1D0V_FB
6	TON		PWR_1D0V_TON
1	PGOOD		PWR_1D0V_PG
4	AGND		
2	EN		PWR_1D0V_EN
19	PGND		
14	PGND		
13	PGND		
12	PGND		
15	PGND		
3	PFM#		PWR_1D0V_PFM
22	SS		PWR_1D0V_SS

PC5204 SCD1U25V2KX-1-DL-GP

PR5203 100KR2F-L1-GP
PC5213 SCD01U50V2KX-1DLGP

Cyntec 7*7*2.4
DCR: 4.5m~5.1mOhm
Idc : 15 A , Isat : 22A

Design Current : 9A
11.25A<OCP>13.5A

PL5201 COIL-D47UH-20-GP

1D0V_PWR
PC5203 PC5205 PC5201 PC5206 PC5208
SC22U6D3V3MX-1-DL-GP
SCD1U25V2KX-1-DL-GP

PG5223 GAP-CLOSE-PWR-6-GP
PWR_1D0V_FB_A

PR5202 2K55R2F-GP
PC5212 SC220P50V2KX-3DLGP
PR5204 10KR2F-2-GP

20170307

Vo=0.8x(1+R1/R2)
=0.8x(1+2.55/10)
=1.004V

3D3V_S5
PR5208 100KR2J-1-GP

40 1D0V_S5_PWRGD
PR5209 0R0402-PAD
PWR_1D0V_PG

17,40,45,54 3V_5V_POK
PR5210 0R0402-PAD
PWR_1D0V_EN

2016/11/25 modify power sequence 2017/03/02

PC5215 SCD1U16V2KX-3GP

<Core Design>

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Eletro-X

SSID = 2D5V/ 1D8V

APL5930 for 2D5V

2017/05/08

PWR_2D5V — PG5401 GAP-CLOSE-PWR-3-GP — 2D5V_S3
PG5402 GAP-CLOSE-PWR-3-GP

3D3V_S5
5V_S5
20161214
PC5410 SC1U10V2KX-1DLGP
PR5410 10KR2F-2-GP
PC5414 SC10U6D3V3MX-DL-GP
Design current = 700mA
PWR_2D5V

51 PWR_2D5V_PG
17,40 SIO_SLP_S4#
PR5417 1 2 0R0402-PAD
PWR_2D5V_EN
PWR_2D5V_FB

PU5403
VCNTL POK EN VIN#9
VIN#5 VOUT#4 VOUT#3 FB GND
APL5930KAI-TRG-GP
74.05930.03D
2ND = 74.G9731.03D

2016/12/30
PR5409 47KR2J-2-GP DY
PC5427 SCD1U25V2KX-1DL-GP DY
20161027

PR5419 29K4R2F-GP R1
PC5411 SC68P50V2JN-1GP DY
PC5413 SC10U25V5KX-DL-GP
PC5412 SC22U6D3V5MX-2GP DY
R2 PR5420 13K7R2F-GP

Vout=0.8V*(R1+R2)/R2

APL5930 for 1D8V_S5

2017/05/08

1D8V_PWR — PG5403 GAP-CLOSE-PWR-3-GP — +V1.8A
PG5404 GAP-CLOSE-PWR-3-GP
PG5405 GAP-CLOSE-PWR-3-GP

5V_S5
20161214
3D3V_S5
PC5401 SC1U10V2KX-1DLGP
PR5402 100KR2F-L1-GP PH at Page40 DY
PC5403 SC10U6D3V3MX-DL-GP
Design Current = 770mA
1D8V_PWR

2017/01/24
24,40 PRIM_PWRGD
17,40,45,52 3V_5V_POK
PR5408 1 2 0R0402-PAD
PR5406 1 2 0R0402-PAD
2017/03/02
PWR_1D8V_POK
PWR_1D8V_EN

PU5401
VCNTL POK EN VIN#9
VIN#5 VOUT#4 VOUT#3 FB GND
APL5930KAI-TRG-GP
74.05930.03D
2ND = 74.G9731.03D

PR5401 47KR2J-2-GP DY
PC5406 SC4700P50V2KX-1GP DY

1.8V_RUN_FB
PR5403 16K5R2F-2-GP R1
PC5405 SC68P50V2JN-1GP DY
PC5404 SC22U6D3V5MX-2GP DY
PC5402 SC10U25V5KX-DL-GP
20161027
R2 PR5404 13K3R2F-L1-GP

Vout=0.8V*(R1+R2)/R2

<Core Design>

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Eletro-X

SSID = LCD

Panel / Camera/ DMIC

2016/11/4

LCD1 — IPEX-CON051-GP

DCBATOUT_LCD

LCDVDD

DBC_EN_R	R5503	0R0402-PAD	DBC_PANEL_EN	20
EDP_AUX	C5510	SCD1U25V2KX-1-DL-GP	EDP_AUX_DP	8
EDP_AUX#	C5511	SCD1U25V2KX-1-DL-GP	EDP_AUX_DN	8
LCD_TST_C				
EDP_TX3#	C5532	SCD1U25V2KX-1-DL-GP	EDP_TX3_DN	8
EDP_TX3	C5531	SCD1U25V2KX-1-DL-GP	EDP_TX3_DP	8
EDP_TX2#	C5533	SCD1U25V2KX-1-DL-GP	EDP_TX2_DN	8
EDP_TX2	C5519	SCD1U25V2KX-1-DL-GP	EDP_TX2_DP	8
EDP_TX1#	C5501	SCD1U25V2KX-1-DL-GP	EDP_TX1_DN	8
EDP_TX1	C5504	SCD1U25V2KX-1-DL-GP	EDP_TX1_DP	8
EDP_TX0#	C5506	SCD1U25V2KX-1-DL-GP	EDP_TX0_DN	8
EDP_TX0	C5509	SCD1U25V2KX-1-DL-GP	EDP_TX0_DP	8
EDP_HPD_CONN				
LCD_BRIGHTNESS				
BLON_OUT_C				

UHD
UHD
UHD
UHD

Camera

3D3V_CAMERA_S0 — For DCBATOUT_CAMERA, For 3D3V_CAMERA_S0

CCD_USB20_CON_P
CCD_USB20_CON_N

IR_CAMERA_DET#_R — R9937 — 0R0402-PAD — IR_CAM_DET# 20 — MIC_GND

DMIC_CLK_C
DMIC_DATA_C

DCBATOUT_CAMERA

020.F0574.0050

2016/12/29 change PN

X02 0414

R5501 0R0402-PAD — MIC_GND

IR CAMERA Power

DCBATOUT_CAMERA — R5520 0R0603-PAD — DCBATOUT

2017/05/08

C5542 SCD1U50V3KX-DL-GP
C5534 SC1KP50V2KX-1DLGP

Sensor/ Touch Panel

TCBD1 — HRS-CON20-9-GP

3D3V_SEN_S0

SENSOR_I2C_SDA	20,70	
SENSOR_I2C_SCL	20,70	
GSEN_INT1	20	
GSEN_INT2	20	
GYRO_INT	70	
GYRO_DRDY	20	
TCH_INTR#	R5523	20R0402-PAD
TCH_I2C_SDA	R5522	20R0402-PAD
TCH_I2C_SCL	R5521	20R0402-PAD

TPAN_VDD

2017/03/02

2016/12/23

Touch Panel

3D3V_S0 — R5504 100KR2J-1-GP

TOUCH_DETECT	20
TOUCH_REPORT_SW	24
TOUCH_PANEL_PD#	4
TOUCH_PANEL_INTR#	4,55
I2C0_SDA_TCH_PNL	20
I2C0_SCL_TCH_PNL	20

2017/04/24

2017/04/24

I2C0_SCL_TCH_PNL — R5517 4K7R2J-2-GP — 3D3V_S0
I2C0_SDA_TCH_PNL — R5518 4K7R2J-2-GP — 3D3V_S0

2IN1_TPNL

020.K0032.0020

2016/11/9

RN5502 SRN100KJ-5-GP

LVDS_VDD_EN_R	
BLON_OUT_C	
BKLT_CTRL	
EDP_HPD_CONN	

LCD_BRIGHTNESS — EC5501 DY C8P50V2DN-1DL-GP — EMI 20160812

2016/12/20 change to 8P DY

8 EDP_VDD_EN — D5501 BAT54C-7-F-3-GP — LVDS_VDD_EN_R
24 LCD_VCC_TEST_EN

75.00054.E7D 2017/05/08

LCDVDD — C5507 SCD1U25V2KX-1-DL-GP — C5508 SC1U10V2KX-1DLGP — R5546 0R0603-PAD — LCDVDD_R — C5505 SC4D7U6D3V3KX-DLGP

Hi:2.0V
Lo:0.8V

LCDVDD Layout 80 mil

U5501 RT9724GB-GP
EN — VIN#5 — 3D3V_S0
GND
VOUT — VIN#4

74.09724.09F
2ND = 74.03514.07F

C5502 SC4D7U6D3V3KX-DLGP

Add 0ohm , 20141118

R5502 0R2J-2-GP DY — D5502 BAT54C-7-F-3-GP — BKLT_CTRL — L_BKLT_CTRL 8 — LCD_TST

75.00054.E7D

DMIC_CLK_C
DMIC_DATA_C
RN5503 SRN33J-5-GP
DMIC_CLK 27
DMIC_DATA 27

EC5503 DY SC3300V2JN-3DLGP — EC5504 SC3300V2JN-3DLGP — 20160812 EMI

R5504,R5505 merge to RN5503
2015/10/06 modify

2017/03/21

LCD_TST_C — R5543 100R2J-2-GP — LCD_TST 24
BLON_OUT_C — R5544 100R2J-2-GP — PANEL_BKEN 27

2016/12/28

LCD_BRIGHTNESS — R5545 100R2J-2-GP — BKLT_CTRL
EDP_HPD_CONN — R5506 100R2J-2-GP — EDP_HPD 8

2016/11/3 **CAMERA POWER**

3D3V_S0 — F5502 POLYSW-1D1A6V-9-GP-U — 3D3V_CAMERA_S0_R — R5513 0R0603-PAD — 3D3V_CAMERA_S0

2016/12/20 — 69.48001.081
2017/05/08 — C5503 SC4D7U6D3V3KX-DLGP

INVERTER POWER

2017/05/08

DCBATOUT — R5514 0R0603-PAD — DCBATOUT_LCD_R — F5503 POLYSW-1D1A24V-GP-U — DCBATOUT_LCD

69.50007.A31
2nd = 69.50007.D31

C5512 SCD1U50V3KX-DL-GP
C5513 SC1KP50V2KX-1DLGP
C5514 SC10U25V5KX-DL-GP

2016/12/21

Starload height limite change to 0603 package
2015/09/24 modify

SENSOR POWER

2017/05/08

3D3V_S0 — F5504 DY POLYSW-1D1A6V-9-GP-U — 3D3V_SEN_S0_R — R5515 0R0603-PAD — 3D3V_SEN_S0

69.48001.081

Add 0603 0ohm , 20141118

EC5506 DY SC33P50V2JN-3GP
C5515 SC4D7U6D3V3KX-DLGP

TOUCH PANEL POWER

2017/05/08

3D3V_S0 — 5V_S0 — F5501 DY POLYSW-1D1A6V-9-GP-U — TPAN_VDD

69.48001.081

R5508 0R0603-PAD
R5509 0R3J-0-GP DY

5V_S0

C5520 DY SCD1U10V3KX-2DLGP
C5523 DY SCD1U10V3KX-2DLGP

U5502 APL5324BI-TRG-GP
VIN — VOUT
GND
SHDN DY — SET

Design Current = 125mA

R5519 31K6R2F-GP DY
R5524 10KR2F-2-GP DY

VOUT=0.8*(1+R1/R2)

C5516 SCD1U50V3KX-DL-GP
C5517 SC1U6D3V3MX-DL-GP
C5518 SC10U6D3V3MX-DL-GP DY

Starload height limite change to 0603 package
2015/09/30 modify

2017/03/17

CCD_USB20_CON_N — EL5501 CCM-900HM-100MHZ-5-GP — CCD_USB20_N 16
CCD_USB20_CON_P — CCD_USB20_P 16

68.00396.001
2nd: = 68.01012.20B

2017/06/12

Touch Panel PH internally. — 3D3V_S0
4,55 TOUCH_PANEL_INTR# — R5505 1 DY 10KR2J-3-GP — R5507 100KR2J-1-GP

2017/03/21

5V_S0 — DY — EC5505 SCD1U50V3KX-DL-GP

TCH_INTR# — 2017/03/17 — ED5502 DY AZ5725-01FDR7G-GP — 83.05725.0A0

ED5501 DY AZ5315-02F-GP
CCD_USB20_CON_P
CCD_USB20_CON_N
2017/03/17
83.05315.0A0

<Core Design>

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Title: LCD&CAM&DMC&Touch
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Eletro-X

SSID = HDMI

2016/11/02modify

2016/11/01modify

2016/12/20

2016/12/14 vendor suggest

2016/11/7modify

2016/11/6modify

2017/03/10

20150116 2037

2017/03/16

20160812 EMI

071.17564.0B0U

PS175HDMBGA64GTR2-B1-GP

72.25200.001

MX25L2006EM1I-12G-GP

082.30008.0361

X5701 XTAL-27MHZ-187-GP

69.48001.081

2nd = 69.50011.081

75.00056.07D

D5701 BAW56-9-GP

022.10025.00M1

SKT-HDMI23-167-GP-U

HDMI CONN

ED5701 L05ESDL5V0NA-4-GP

ED5702 L05ESDL5V0NA-4-GP

<Core Design>

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Title: HDMI

Size: A2 | Document Number: KyloRen 13" | Rev: A00

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Eletro-X

SSID = HDMI

AOZ2023 for HDMI 1D2V

Design Current = 550mA

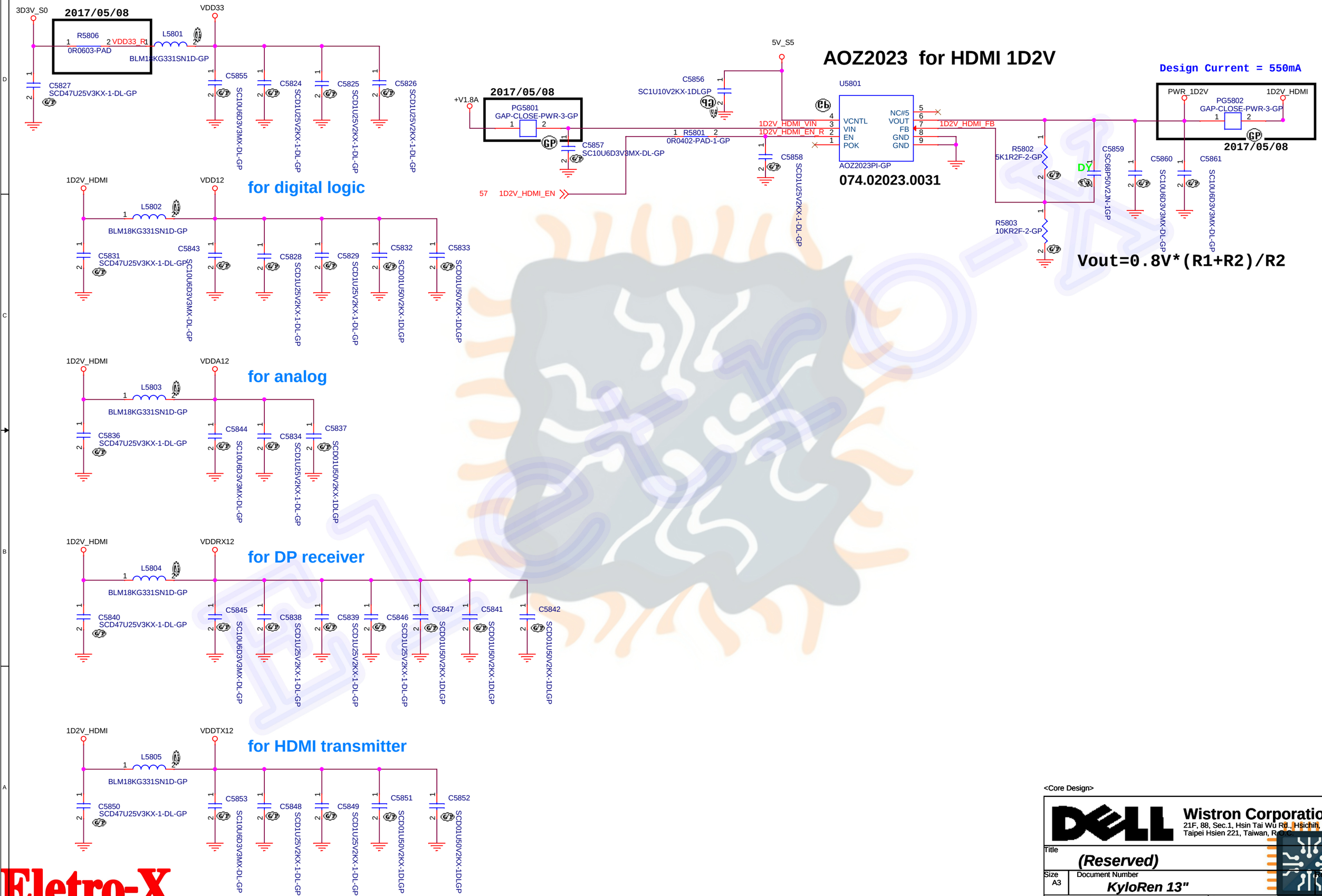
for digital logic

for analog

for DP receiver

for HDMI transmitter

Vout=0.8V*(R1+R2)/R2



<Core Design>

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Title: *(Reserved)*

Size: A3 | Document Number: *KyloRen 13"* | Rev: *A00*

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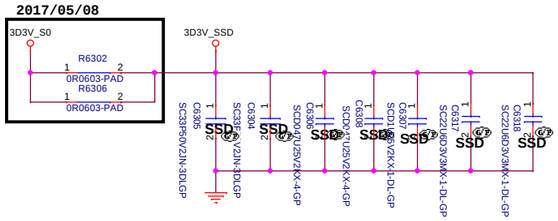
Eletro-X

SSID = M.2

2017/05/08



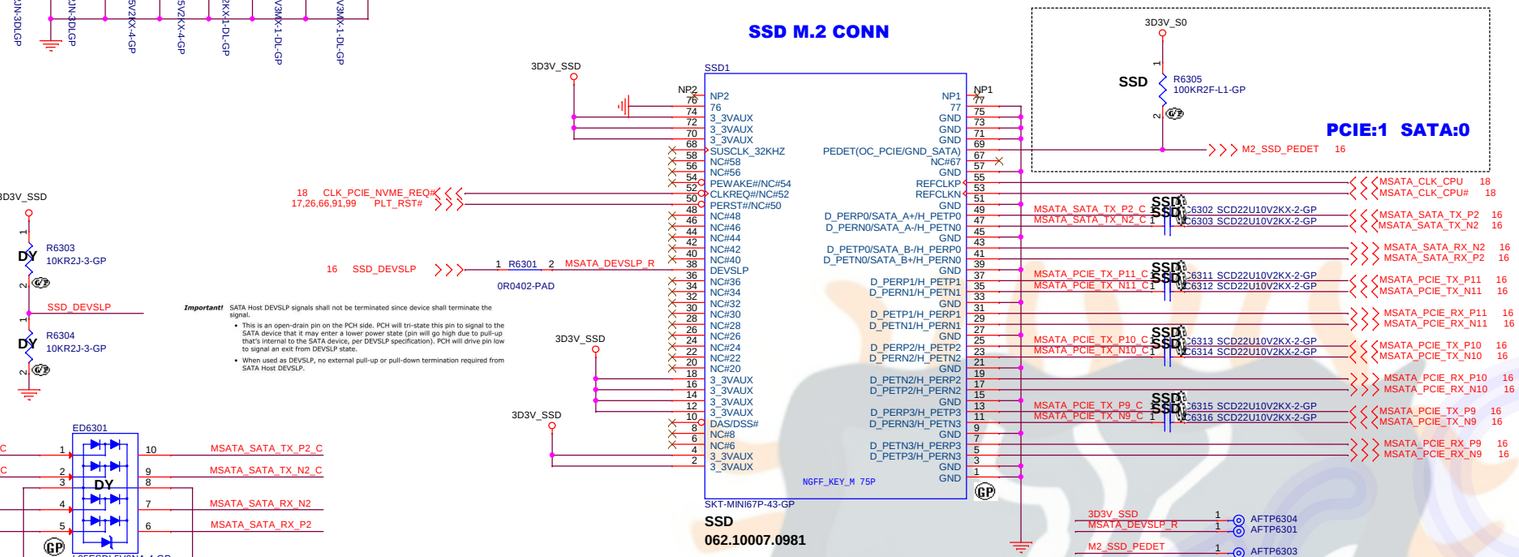


Table 13-11. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Eletro-X

<Core Design>

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Title: (Reserved)

Size: A2 | Document Number: KyloRen 13" | Rev: A00

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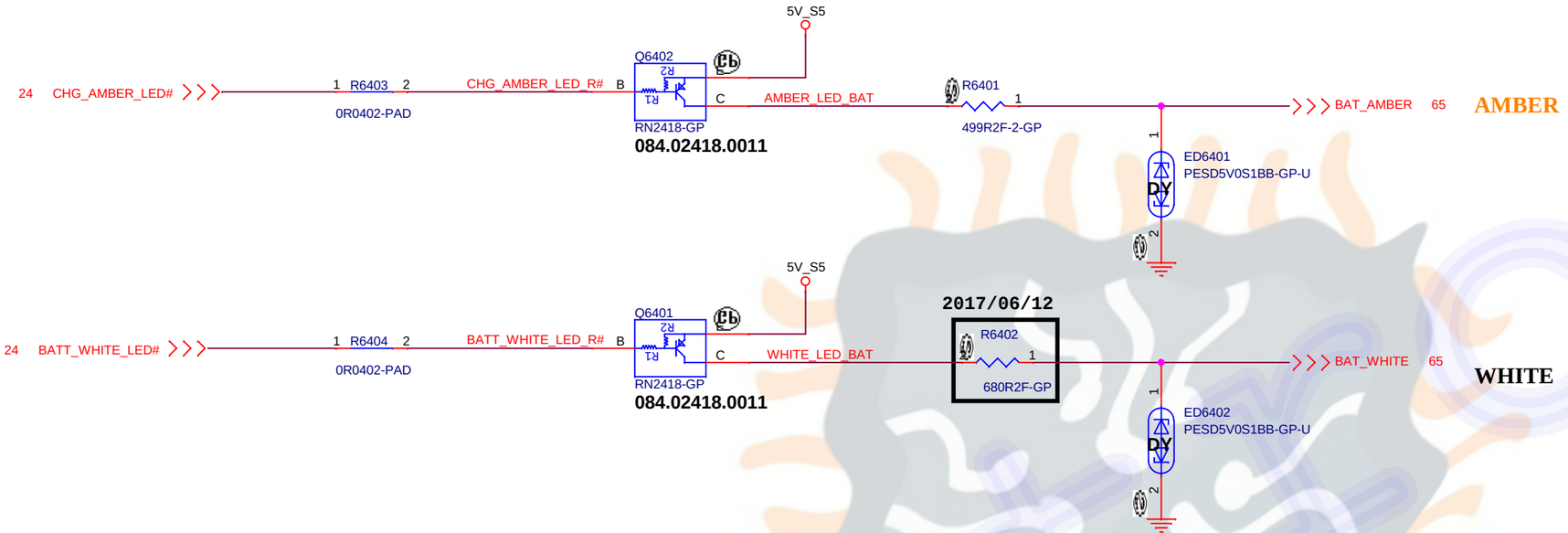
SSID = Power BTN

Battery LED1 (AMBER_LED)

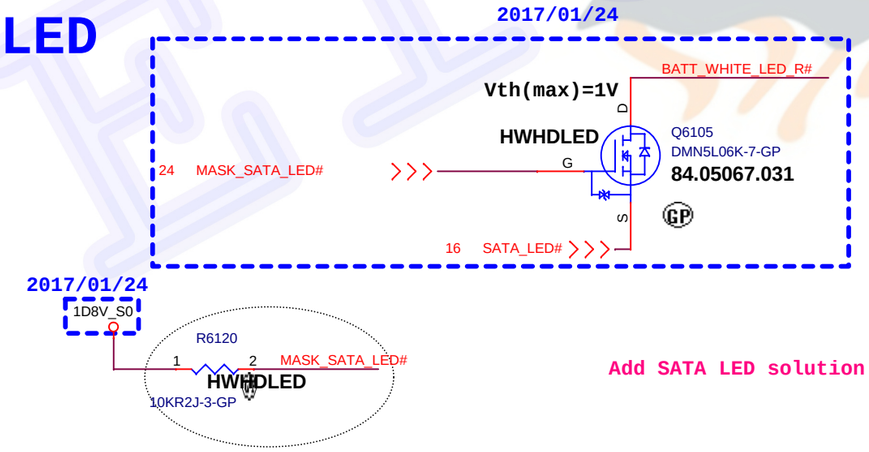
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

SATA LED



Add SATA LED solution by customer request 2016/02/03

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Board&Power Button

Size: A3 | Document Number: KyloRen 13" | Rev: A00

Date: Thursday, June 29, 2017 | Sheet 64 of 106

Eletro-X

SSID = KB

Keyboard

24 KSI[0..7]

24 KSO[0..16]

KBBD1

20 KB_DET#

AFTP6502 KSI7
AFTP6503 KSI6
AFTP6505 KSI4
AFTP6508 KSI2
AFTP6506 KSI5
AFTP6501 KSI1
AFTP6509 KSI3
AFTP6512 KSI0
AFTP6510 KSO5
AFTP6514 KSO4
AFTP6515 KSO7
AFTP6517 KSO6
AFTP6516 KSO8
AFTP6518 KSO3
AFTP6511 KSO1
AFTP6513 KSO2
AFTP6507 KSO0
AFTP6519 KSO12
AFTP6539 KSO16
AFTP6524 KSO15
AFTP6520 KSO13
AFTP6521 KSO14
AFTP6504 KSO9
AFTP6522 KSO11
AFTP6523 KSO10

CAP_LED
AFTP6538

PTWO-CON30-18-GP
020.K0210.0030

2016/12/07 change PN

+5V_KB_BL
C6506 SCD1U16V2KX-3DLGP
KB_LED_DET_C
KB_BL_CTRL#
KBBL1
ACES-CON4-90-GP-U
020.K0298.0004

2016/11/3

TP_VDD
C6505 SCD1U25V2KX-1-DL-GP
4.24
TP_WAKE_KBC#
24 PTP_DIS#
I2C0_SDA_R
I2C0_SCL_R
TPDATA_C
TPCLK_C
AFTP6525
TP1
PTWO-CON8-16-GP
020.K0255.0008

2016/12/28 change PN

LED1
64 BAT_AMBER
64 BAT_WHITE
PTWO-CON4-21-GP
020.K0255.0004
2016/12/28 change PN
?

5V_S0
F6501 POLYSW-D5A6V-1-GP
+5V_KB_BL_R
2017/05/08
R6501 0R0603-PAD
+5V_KB_BL
KBBL
69.50007.921
C6501 SCD1U25V2KX-1-DL-GP

KB Backlight Power Consumption: 285mA max.

KB_BL_CTRL#
2016/10/31modify
24 KB_LED_PWM
Q6501 DMN3404L-7-1-GP
084.03404.0A31
R6509 100KR2J-1-GP
19 KB_LED_BL_DET
R6507 51KR2J-1-GP
KB_LED_DET_C
R6508 100KR2J-1-GP
C6504 SCD1U16V2KX-3DLGP
+5V_KB_BL
AFTP6529
KB_BL_CTRL#
AFTP6530

CAP LED Control
LOW actived from KBC GPIO

X02 0414
24 CAP_LED#_R
R6512 0R0402-PAD
CAP_LED_R#
Q6505 RN2418-GP
5V_S5
CAP_LED_Q
R6513
CAP_LED
1KR2J-1-GP
084.02418.0011

SSID = TPAD

3D3V_S5
3D3V_S0
TP_VDD
TP_WAKE
Q6502 DMP2130L-7-GP
NON TP_WAKE
R6502 0R3J-0-U-GP
C6502 SCD1U25V2KX-1-DL-GP
R6514 0R0603-PAD
84.02130.031
2ND = 84.03413.A31
2017/05/08
24 TP_EN#
TP_ON#_GATE
R6504 20KR2F-L-GP
?

TP_VDD Discharge Circuit
TP_VDD
TP_ON#_GATE
Q6503
TP_WAKE
R6503 100R3J-4-GP
Q6205_Q
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31
4th = 84.2N702.W31

GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)

TP_VDD
RN6501 SRN10KJ-5-GP

PS2
I2C

24 CLK_TP_SIO
24 DAT_TP_SIO
20 I2C0_SCL_TCH_PAD
20 I2C0_SDA_TCH_PAD
RN6502 SRN33J-5-GP-U
TPCLK_C
TPDATA_C
0R2J-2-GP
NON TP_WAKE
R6505 I2C0_SCL_R
R6506 I2C0_SDA_R
EC6501 SC33P50V2JN-3DLGP
EC6502 SC33P50V2JN-3DLGP
EC6503 SC33P50V2JN-3DLGP
EC6504 SC33P50V2JN-3DLGP
20160812 EMI
DY DY DY DY

5V_S0
A00 0609
R6510 0R0402-PAD
TP_VDD
RN6503 SRN2K2J-1-GP
TP_WAKE
Q6204_G
Q6504 2N7002KDW-GP
I2C0_SCL_TCH_PAD
I2C0_SDA_TCH_PAD
I2C0_SCL_R
I2C0_SDA_R
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

X02 0415
TP_VDD
R6511 10KR2J-3-GP
TP_WAKE_KBC#

Change pindefine DVT1 0210 1330

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

TP_VDD 1 AFTP6531
TPCLK_C 1 AFTP6532
TPDATA_C 1 AFTP6533
I2C0_SCL_R 1 AFTP6534
I2C0_SDA_R 1 AFTP6535
TP_WAKE_KBC# 1 AFTP6536
PTP_DIS# 1 AFTP6537

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board&Touch Pad
Size: A2
Document Number: KyloRen 13"
Rev: A00
Date: Thursday, June 29, 2017
Sheet 65 of 86

Eletro-X

SSID = IO Connector

2016/11/07

IOBD1

51 53 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 54 52

STAR-CON50-2-GP-U

020.F0688.0050

WLAN

WLAN_PCIE_TX_P 16
WLAN_PCIE_TX_N 16
WLAN_PCIE_RX_N 16
WLAN_PCIE_RX_P 16

IO board USB3.0

USB2_USB30_TX_P3 16
USB2_USB30_TX_N3 16
USB2_USB30_RX_P3 16
USB2_USB30_RX_N3 16

WLAN_CLK_CPU 18
WLAN_CLK_CPU# 18

Card Reader

CARD1_USB20_CON_P
CARD1_USB20_CON_N

BT

BT_USB20_CON_N
BT_USB20_CON_P

2016/11/09

USB3.0 port3

USB2_USB20_CON_P
USB2_USB20_CON_N

5V_S5

3D3V_WLAN

2017/05/02

3D3V_S5

+RTC_VCC

BREATH_LED# 24
PLT_RST# 17,26,63,91,99
CLK_PCIE_WLAN_REQ# 18

KBC_PWRBTN# 24

WIFI_RF_EN 15
BLUETOOTH_EN 20
USB_OC1# 16
USB_EN# 24,35

C6605
DY
SCD1U16V2KX-3DLGP

CARD1_USB20_CON_P 1 AFTP6601
CARD1_USB20_CON_N 1 AFTP6602
BT_USB20_CON_P 1 AFTP6603
BT_USB20_CON_N 1 AFTP6604
USB2_USB20_CON_P 1 AFTP6605
USB2_USB20_CON_N 1 AFTP6606
3D3V_S5 1 AFTP6607
5V_S5 1 AFTP6608

2016/12/07 add AFTP

KBC_PWRBTN# 1 AFTP6609

2016/12/16 add AFTP

Change choke Height just for Starload
2015/09/23 modify

EL6601

USB2_USB20_CON_P 1 2 USB2_USB20_P 16
USB2_USB20_CON_N 4 3 USB2_USB20_N 16

COIL-90OHM-100MHZ-3-GP

68.00396.001

2nd: = 68.01012.20B

EL6602

CARD1_USB20_CON_P 1 2 CARD1_USB20_P 16
CARD1_USB20_CON_N 4 3 CARD1_USB20_N 16

COIL-90OHM-100MHZ-3-GP

68.00396.001

2nd: = 68.01012.20B

BT_USB20_CON_N R6605 1 2 BT_USB20_N 16
BT_USB20_CON_P R6606 1 2 BT_USB20_P 16

0R0402-PAD
0R0402-PAD

2017/03/16

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

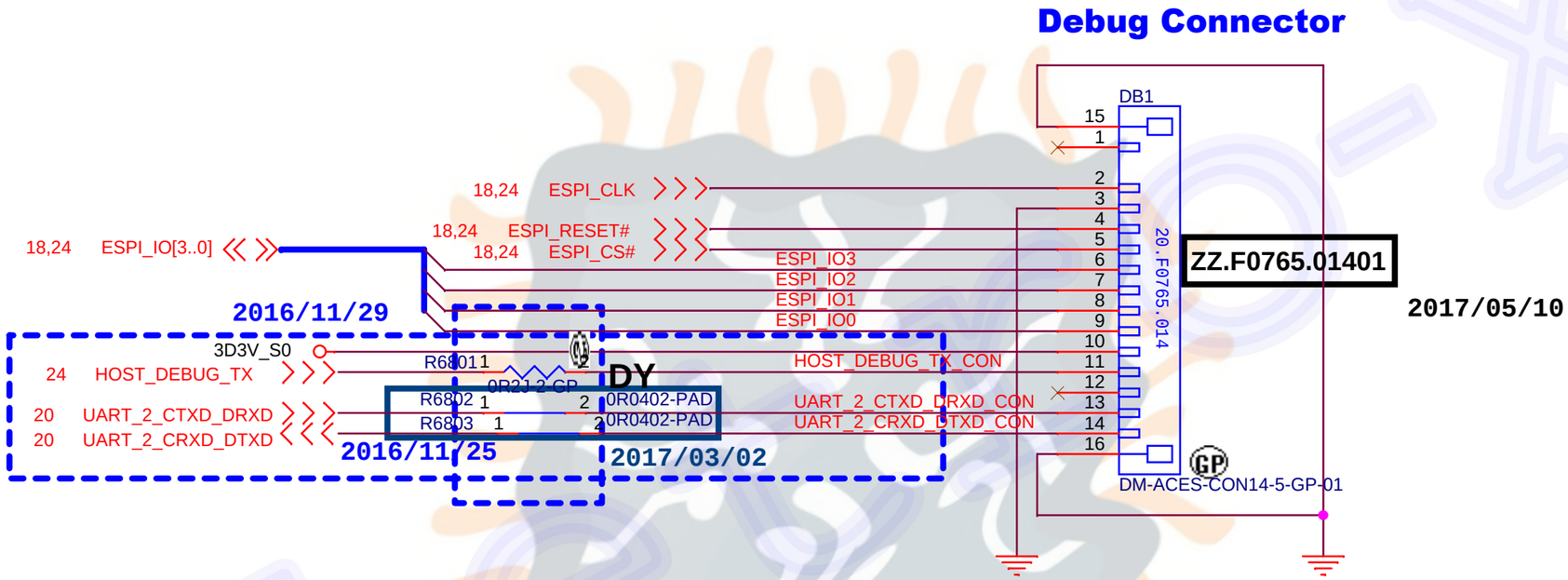
Size: A3 | Document Number: KyloRen 13" | Rev: A00

Date: Thursday, June 29, 2017 | Sheet 66 of 106

Eletro-X

SSID = Debug

Debug Connector



Use ZZ.F0765.01401 DUMMY PAD for MP

<Core Design>

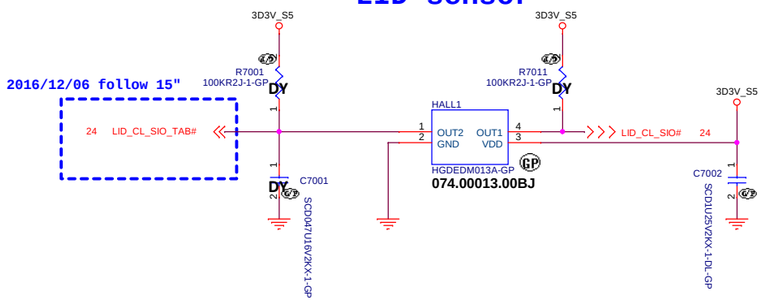
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Dubug connector*	
Size A4	Document Number *KyloRen 13"*	Rev A00
Date: Thursday, June 29, 2017	Sheet 68 of 106	

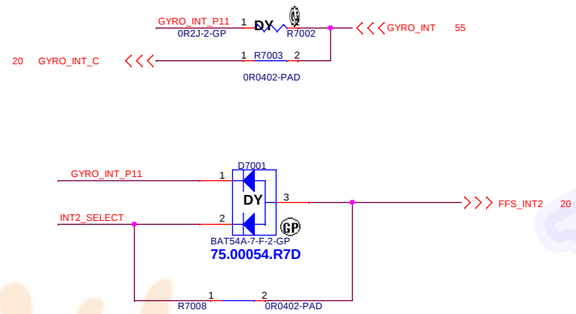
Eletro-X

SSID = Hall Sensor

LID sensor

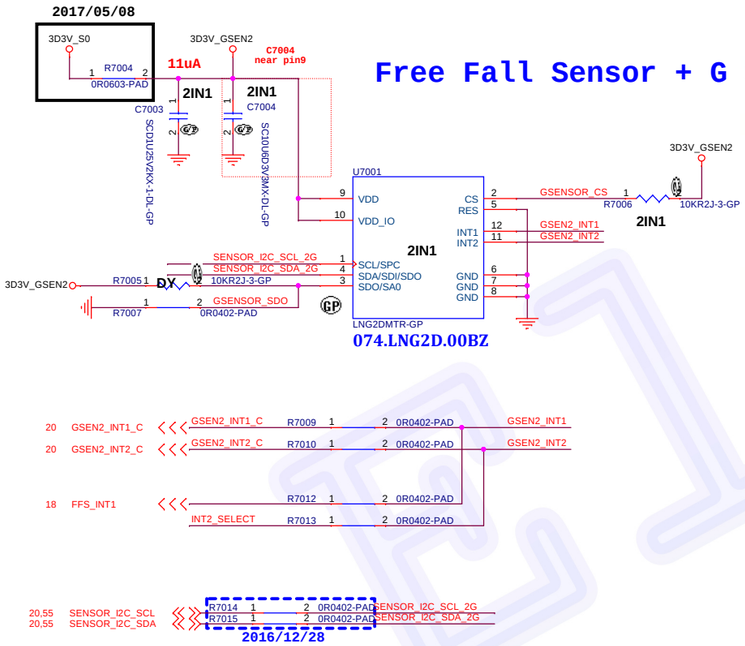


combine G



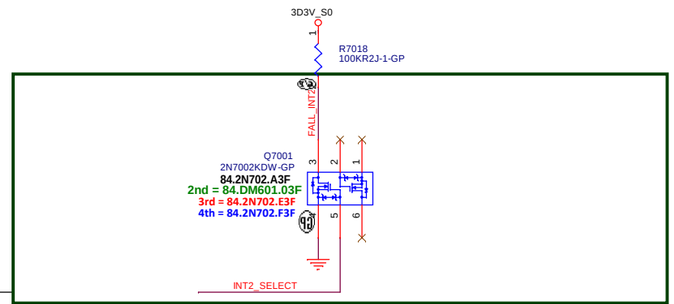
Note:
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Free Fall Sensor + G Sensor



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

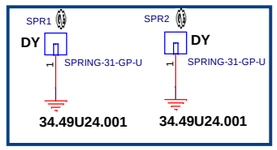
Please help to close with U6602



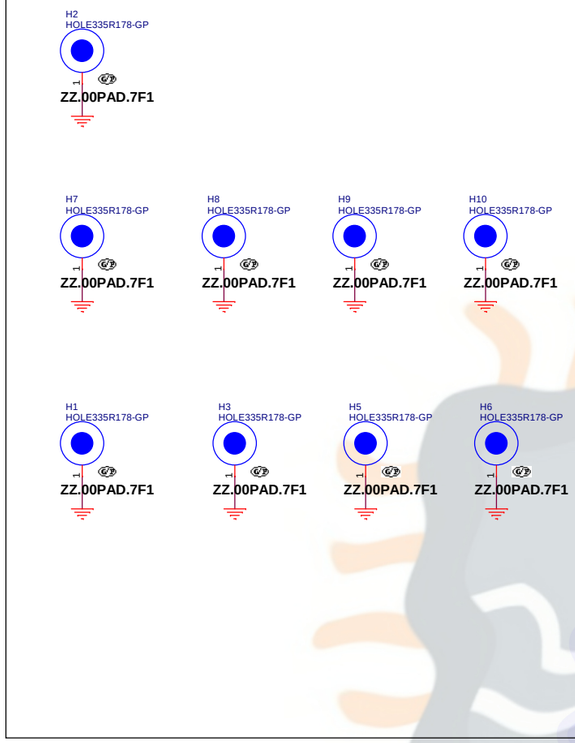
Eletro-X

SSID = Unused Parts

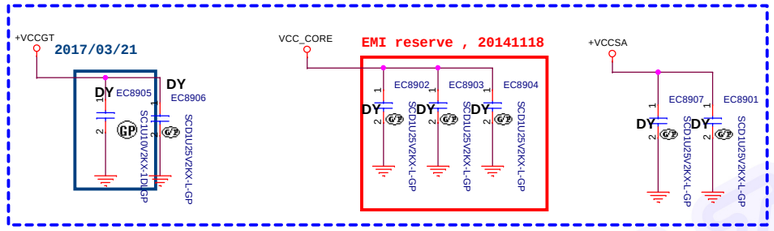
34.4YW18.001



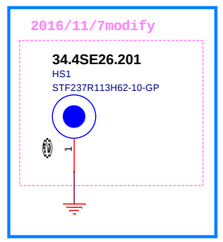
ZZ.00PAD.7F1



2016/12/14 move from P.10 to P.89

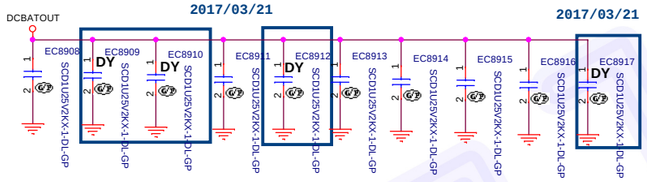


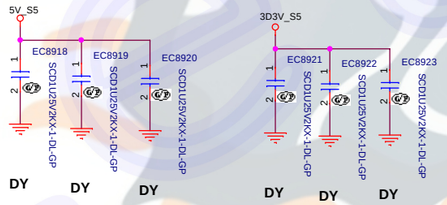
Type-C

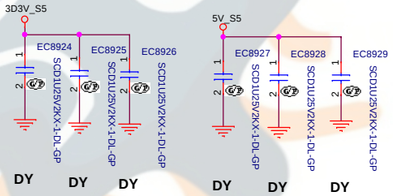


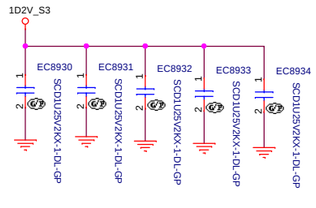
SSID = EMI

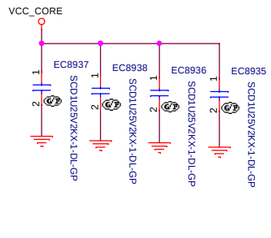
Mind the voltage rating of the caps.



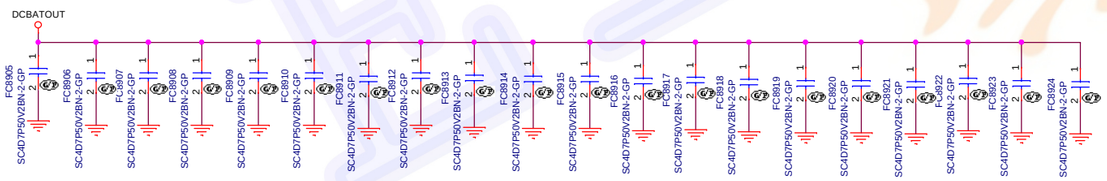


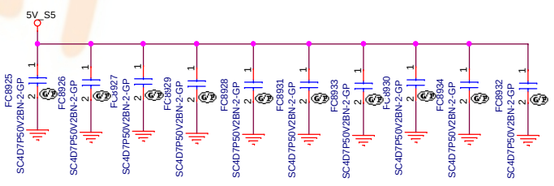


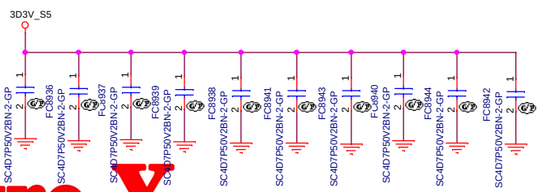


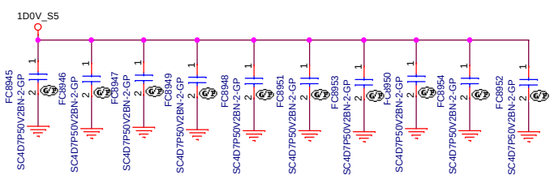


SSID = RF









Eletro-X

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A2
Document Number: KyloRen 13"
Rev: 1.00
Date: Thursday, June 29, 2017
Sheet 89 of 89

SSID = TPM

3D3V_TPM
R9140 1 TPM2 2 10KR2J-3-GP

18 SPI_CS_ROM_N2
18,25 SPI_SO_ROM
18,25 SPI_SI_ROM
18,25 SPI_CLK_ROM

R9130 1 TPM2 2 0R2J-2-GP SPI_CS2#_R_TPM2
R9132 1 TPM2 2 33R2J-2-GP SPI_SO_ROM_TPM2
R9133 1 TPM2 2 33R2J-2-GP SPI_SI_ROM_TPM2
R9138 1 TPM2 2 33R2J-2-GP SPI_CLK_ROM_TPM2

3D3V_TPM
R9125 1 DY 2 10KR2J-3-GP
TPM_GPIO2

Q9103
S
G
D
DY
SPI_CS_ROM_N1
2N7002K-2-GP
84.2N702.J31

Q9102
DMP2130L-7-GP
3D3V_TPM
TPM_GPIO2
D
G
S
DY
84.02130.031
R9124 1 DY 2 10KR2J-3-GP
Q9102.G 1 R9123 2 SPI_CS_ROM_N1
DY
100R2F-L1-GP-U

3D3V_TPM
R9149 2 DY 1 SPI_IRQ#_TPM2
10KR2J-3-GP
If not used, it is ok to left it unconnected

2016/11/03

3D3V_S5_PCH
R9143 TPM2 1
D01R3F-L-GP
3D3V_TPM
C9106 1 TPM2 2 SC4D7U6D3V3KX-DLGP
R9144 TPM2 0R3J-0-U-GP
C9108 1 TPM2 2 SCD1U16V2KX-3DLGP

3D3V_S0
R9145 2 TPM2 1 0R3J-0-U-GP
3D3V_S5_PCH
R9146 2 DY 1 0R3J-0-U-GP
+UZ12_TPM
C9109 1 TPM2 2 SC4D7U6D3V3KX-DLGP

TPM_VSB
3D3V_TPM
R9147 2 TPM2 1 0R3J-0-U-GP TPM_VDD14
R9148 2 TPM2 1 0R3J-0-U-GP TPM_VDD22
C9110 1 TPM2 2 SCD1U16V2KX-3DLGP

2017/05/08

18 TPM_SPI_IRQ#
R9137 1 TPM2 2 0R2J-2-GP SPI_IRQ#_TPM2
17,26,63,66,99 PLT_RST#
R9136 1 TPM2 2 0R2J-2-GP PLT_RST#_Q_TPM2

R9141 1 TPM2 2 10KR2J-3-GP

EV Reseved for modern stanby

17,24,40 SIO_SLP_S0#
2 DY 1 R9142 0R2J-2-GP

U9102
+UZ12_TPM 8 VDD
TPM_VSB 1 VSB
VHIO 14
VHIO 22
SPI_SO_ROM_TPM2 24
SPI_SI_ROM_TPM2 21
SPI_IRQ#_TPM2 18
LAD3 15
PLT_RST#_Q_TPM2 17
SPI_CLK_ROM_TPM2 19
SPI_CS2#_R_TPM2 20
SERIRQ_TPM 27
SERIRQ 28
LPCPD# 4
PP 5
TEST 12
RESERVED
LAD0/MISO
LAD1/MOSI
LAD2/SPI_IRQ#
LRESET#/SPI_RST#/SRESET#
LCLK/SCLK
LFRAME#/SCS#
TPM2
NPCT650JB2YX-GP
071.00650.0J03

SDA/GPIO0 29 TPM_GPIO0
GPIO1/SCL 30 TPM_GPIO2
GPX/GPIO2 3 TPM_GPIO2
GPIO3/BADD 6 TPM_GPIO4
CLKRUN#/GPIO4/SINT# 13 TPM_GPIO4

R9121 1 TPM2 2 10KR2J-3-GP
R9120 1 DY 2 10KR2J-3-GP
R9122 1 DY 2 0R3J-0-U-GP SPI_CS_ROM_N1
3D3V_S0

NC#2 2
NC#7 7
NC#10 10
NC#11 11
NC#25 25
NC#26 26
NC#31 31

GND 9
GND 16
GND 23
GND 32
GND 33
GND

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPM2.0
Size: A3
Document Number: KyloRen 13"
Rev: A00
Date: Thursday, June 29, 2017
Sheet 91 of 106

Eletro-X

SSID = FPR

FBR(finger Print Sensor)

2016/12/23

3D3V_S0

3D3V_S5

2016/11/03

R9204 D01R3F-L-GP

FPR

R9203 0R3J-0-U-GP

DY

FPR_VDD1

2016/12/09

C9907 SC1U10V2KX-1DLGP

FPR

FPR1

FPR

020.K0237.0006

HRS-CON8-GP

FP1_USB20_CON_N

FP1_USB20_CON_P

16 FP1_USB20_N

R9205 0R2J-2-GP FPR FP1_USB20_R_N

16 FP1_USB20_P

R9207 0R2J-2-GP FPR FP1_USB20_R_P

R9206 0R2J-2-GP PWFPR BFP1_USB20_R_N

R9208 0R2J-0-GP PWFPR BFP1_USB20_R_P

2016/12/15

FP1_USB20_R_P

R9202 0R2J-2-GP FPR FP1_USB20_CON_P

2017/03/16

FP1_USB20_R_N

R9201 0R2J-2-GP FPR FP1_USB20_CON_N

ED9201

FPR

AZ5315-02F-GP

FP1_USB20_CON_N

FP1_USB20_CON_P

83.05315.0A0

FBR(Botton side finger Print Sensor)

2016/12/23

3D3V_S0

3D3V_S5

2017/05/10

D9201 RB751V-40H-GP

DY

83.R2004.G8F

R9211 0R3J-0-U-GP

PWFPR

R9212 0R3J-0-U-GP

DY

FPR_VDD2

2016/12/09

C9908 SC1U10V2KX-1DLGP

PWFPR

FPR2

PWFPR

PTWO-CON8-11-GP

20.K0767.008

BFP1_USB20_CON_N

BFP1_USB20_CON_P

FPR_SCAN# 24

2017/03/14

BFP1_USB20_R_N

R9209 0R2J-2-GP PWFPR BFP1_USB20_CON_N

2017/03/16

BFP1_USB20_R_P

R9210 0R2J-2-GP PWFPR BFP1_USB20_CON_P

ED9202

PWFPR

AZ5315-02F-GP

BFP1_USB20_CON_N

BFP1_USB20_CON_P

83.05315.0A0

<Core Design>

Wistron Corporation
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SSID = Debug

CPU XDP

Layout Note:
ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG<0>

CFG0 — R9907 1KR2J-1-GP (DY) — FIVR_EN_R

Layout Note:
ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG<3>

CFG3 — R9902 1KR2J-1-GP (XDP) — XDP_PRSNT_PIN1

17,24 PCH_RSMRST# — R9904 1KR2J-1-GP (XDP)
17 H_VCCST_PWRGD — R9903 1KR2J-1-GP (DY)
→ PM_RSMRST_PWRGD_XDP

17,24 SYS_PWROK — R9908 0R2J-2-GP (DY)

3D3V_S5 — R9909 1K5R2J-3-GP (DY) — SPI_SI_XDP — R1828 1KR2J-1-GP (DY)

PLACE WITHIN 1.1 INCH OF PCH
SPI_SI_XDP — R1826 (DY) 1KR2J-1-GP — PCH_SPI_SI — TP1021
(#543016)Optional, can be left as OPEN/No-Connect.

XDP_PREQ# — C9901 SCD1U16V2KX-3DLGP (DY) — 11/27 JAIME

1V_XDP_S5 — R9934 51R2J-2-GP (DY)

16 XDP_PREQ#
16 XDP_PRDY#

XDP1 (XDP)
NP1 / NP2
XDP_PRSNT_PIN1
CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17 CFG18 CFG19
4 XDP_BPM0
4 XDP_BPM1
PM_RSMRST_PWRGD_XDP
+V1.00A_CPU_XDP_AB
FIVR_EN_R
SPI_SI_XDP
XDP_TCLK1
XDP_TCLK
XDP_TDO
SPI_WP_XDP
PCIE_CLK_XDP_P 18
PCIE_CLK_XDP_N 18
TP_PMODE_XDP_RST_R_N
XDP_TRST# 4
PCH_JTAG_TDI 4
PCH_JTAG_TMS 4
R1827 1KR2J-1-GP (XDP) — SPI_WP_ROM 18,25

17,24 SIO_PWRBTN#
(#543016)Routing of this signal to CFG[0] is OPTIONAL.

C9903 SCD1U25V2KX-1-DL-GP (XDP)
18 PCH_SMBDATA
18 PCH_SMBCLK

6 CFG[19:0] → CFG[19:0]

PAD-60P-GP (GP) ZZ.00PAD.Q81 2017/05/08

EE Note:
Use ZZ.00PAD.Q81 DUMMY PAD for MP.

01/30 JAIME
PLACE WITHIN 1.1INCH NEAR CPU XDP CONNECTOR

1D0V_S5 — R9901 0R2J-2-GP (XDP) — 1V_XDP_S5 — R9905 0R2J-2-GP (XDP) — +V1.00A_CPU_XDP_AB
C9902 SCD1U16V2KX-3DLGP (DY) Close to Pin43
PH in P.17

C9905 SCD1U25V2KX-1-DL-GP (XDP) — XDP_DBRESET# 17

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

(#544669)
XDP_TCLK1 — R9914 0R2J-2-GP (XDP) — PCH_JTAG_TCK 4
XDP_TCLK — R9915 0R2J-2-GP (XDP) — XDP_TCK_JTAGX 4
XDP_TDO — R9920 0R2J-2-GP (XDP) — PCH_JTAG_TDO 4
01/27 JAIME

+VCCIO — R9906 150R2J-L1-GP-U (DY) — FIVR_EN_R

01/27 JAIME

1V_XDP_S5 — R9932 1K5R2J-3-GP (XDP)
6 ITP_PMODE
(#544669 Rev0.52) NC.
R9933 0R2J-2-GP (XDP) — TP_PMODE_XDP_RST_R_N
17,26,63,66,91 PLT_RST# — R9930 1KR2J-1-GP (DY)

3D3V_S5 — R9936 3KR2J-2-GP (XDP)
18 SPI_SI_XDP

C9906 SCD1U25V2KX-1-DL-GP (XDP)

<Core Design>

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Change notes -

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